US009362494B2

(12) **United States Patent**
Pellizzer et al.

(10) **Patent No.: US 9,362,494 B2**
(45) **Date of Patent: Jun. 7, 2016**

(54) **ARRAY OF CROSS POINT MEMORY CELLS AND METHODS OF FORMING AN ARRAY OF CROSS POINT MEMORY CELLS**

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventors: **Fabio Pellizzer**, Boise, ID (US); **Stephen W. Russell**, Boise, ID (US); **Tony M. Lindenberg**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/293,577**

(22) Filed: **Jun. 2, 2014**

(65) **Prior Publication Data**

US 2015/0349255 A1 Dec. 3, 2015

(51) **Int. Cl.**
H01L 45/00 (2006.01)
H01L 27/24 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 45/1233*** (2013.01); ***H01L 27/2463*** (2013.01); ***H01L 45/04*** (2013.01); ***H01L 45/06*** (2013.01); ***H01L 45/144*** (2013.01); ***H01L 45/146*** (2013.01); ***H01L 45/147*** (2013.01); ***H01L 45/1675*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,752,118 A 6/1988 Johnson
4,849,247 A 7/1989 Scanlon et al.
4,987,099 A 1/1991 Flanner
5,055,423 A 10/1991 Smith et al.
5,166,758 A 11/1992 Ovshinsky et al.
5,341,328 A 8/1994 Ovshinsky et al.
5,895,963 A 4/1999 Yamazaki
5,912,839 A 6/1999 Ovshinsky et al.
6,143,670 A 11/2000 Cheng et al.
6,611,453 B2 8/2003 Ning
6,613,604 B2 9/2003 Maimon et al.
6,661,330 B1 12/2003 Young

(Continued)

FOREIGN PATENT DOCUMENTS

EP 12850697.9 6/2015
WO WO 2005/041196 5/2005

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 14/242,588, filed Apr. 1, 2014, Lindenberg.

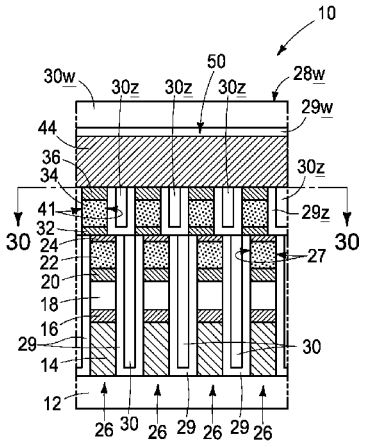
(Continued)

Primary Examiner — Duy T Nguyen
Assistant Examiner — Bo Bin Jang
(74) *Attorney, Agent, or Firm* — Wells St. John, P.S.

(57) **ABSTRACT**

An array of cross point memory cells comprises spaced elevationally inner first lines, spaced elevationally outer second lines which cross the first lines, and a multi-resistive state region elevationally between the first and second lines where such cross. Individual of the multi-resistive state regions comprise elevationally outer multi-resistive state material and elevationally inner multi-resistive state material that are electrically coupled to one another. The inner multi-resistive state material has opposing edges in a vertical cross-section. The outer multi-resistive state material has opposing edges in the vertical cross-section that are laterally offset relative to the opposing edges of the inner multi-resistive state material in the vertical cross-section. Methods are also disclosed.

24 Claims, 15 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

6,664,182 B2 12/2003 Jeng
6,692,898 B2 2/2004 Ning
6,700,211 B2 3/2004 Gonzalez
6,764,894 B2 7/2004 Lowrey
6,815,704 B1 11/2004 Chen
7,148,140 B2 12/2006 Leavy et al.
7,169,624 B2 1/2007 Hsu
7,332,401 B2 2/2008 Moore et al.
7,422,926 B2 9/2008 Pellizzer et al.
7,453,111 B2 11/2008 Ryoo et al.
7,619,933 B2 11/2009 Sarin
7,638,787 B2 12/2009 An et al.
7,646,631 B2 1/2010 Lung
7,719,039 B2 5/2010 Muralidhar et al.
7,772,680 B2 8/2010 Manning
7,773,413 B2 8/2010 Shalvi
7,785,978 B2 8/2010 Smythe
7,800,092 B2 9/2010 Liu et al.
7,803,655 B2 9/2010 Johnson et al.
7,838,341 B2 11/2010 Dennison
7,867,832 B2 1/2011 Yang et al.
7,888,711 B2 2/2011 Cheung et al.
7,915,602 B2 3/2011 Sato
7,919,766 B2 4/2011 Lung
7,935,553 B2 5/2011 Scheurlein et al.
7,974,115 B2 7/2011 Jeong et al.
8,013,319 B2 9/2011 Chang
8,110,822 B2 2/2012 Chen
8,486,743 B2 7/2013 Bresolin et al.
8,507,353 B2 8/2013 Oh et al.
8,546,231 B2 10/2013 Pellizzer et al.
8,614,433 B2 12/2013 Lee et al.
8,723,155 B2 5/2014 Redaelli et al.
8,765,555 B2 7/2014 Van Gerpen
8,822,969 B2 9/2014 Hwang
2002/0017701 A1 2/2002 Klersy et al.
2002/0173101 A1 11/2002 Shau
2002/0177292 A1 11/2002 Dennison
2004/0178425 A1 9/2004 Kato
2004/0188668 A1 9/2004 Hamann et al.
2005/0006681 A1 1/2005 Okuno
2005/0110983 A1 5/2005 Jeong et al.
2005/0117397 A1 6/2005 Morimoto
2006/0073652 A1 4/2006 Pellizzer et al.
2006/0076548 A1 4/2006 Park et al.
2006/0113520 A1 6/2006 Yamamoto et al.
2006/0157682 A1 7/2006 Scheurlein
2006/0186440 A1 8/2006 Wang et al.
2006/0284279 A1 12/2006 Lung et al.
2006/0286709 A1 12/2006 Lung et al.
2007/0008773 A1 1/2007 Scheurlein
2007/0012905 A1 1/2007 Huang
2007/0029676 A1 2/2007 Takaura et al.
2007/0054486 A1 3/2007 Yang
2007/0075347 A1 4/2007 Lai et al.
2007/0075359 A1 4/2007 Yoon et al.
2007/0108431 A1 5/2007 Chen et al.
2007/0158698 A1 7/2007 Dennison et al.
2007/0224726 A1 9/2007 Chen et al.
2007/0235708 A1 10/2007 Elmgreen et al.
2007/0279974 A1 12/2007 Dennison et al.
2008/0043520 A1 2/2008 Chen
2008/0054470 A1 3/2008 Amano et al.
2008/0067485 A1 3/2008 Besana et al.
2008/0067486 A1 3/2008 Karpov et al.
2008/0093703 A1 4/2008 Yang et al.
2008/0101109 A1 5/2008 Haring-Bolivar et al.
2008/0105862 A1 5/2008 Lung et al.
2008/0123394 A1* 5/2008 Lee G11C 11/16 365/148
2008/0128677 A1 6/2008 Park et al.
2008/0137400 A1 6/2008 Chen et al.
2008/0138929 A1 6/2008 Lung
2008/0157053 A1 7/2008 Lai et al.
2008/0197394 A1 8/2008 Caspary et al.
2009/0008621 A1 1/2009 Lin et al.
2009/0017577 A1 1/2009 An et al.
2009/0032794 A1 2/2009 Hsiao
2009/0039333 A1 2/2009 Chang et al.
2009/0072213 A1 3/2009 Elmgreen et al.
2009/0072341 A1 3/2009 Liu et al.
2009/0091971 A1 4/2009 Dennison et al.
2009/0101883 A1 4/2009 Lai et al.
2009/0108247 A1 4/2009 Takaura et al.
2009/0115020 A1 5/2009 Yang et al.
2009/0127538 A1 5/2009 Ryoo et al.
2009/0147564 A1 6/2009 Lung
2009/0166601 A1 7/2009 Czubatyj et al.
2009/0194757 A1 8/2009 Lam et al.
2009/0194758 A1 8/2009 Chen
2009/0230505 A1 9/2009 Dennison
2009/0298222 A1 12/2009 Lowrey et al.
2009/0302300 A1 12/2009 Chang
2009/0321706 A1 12/2009 Happ et al.
2010/0001248 A1 1/2010 Wouters et al.
2010/0001253 A1 1/2010 Arnold et al.
2010/0019221 A1 1/2010 Lung et al.
2010/0054029 A1 3/2010 Happ et al.
2010/0055830 A1 3/2010 Chen et al.
2010/0065530 A1 3/2010 Walker et al.
2010/0072447 A1 3/2010 Lung
2010/0072453 A1 3/2010 Jeong et al.
2010/0107403 A1 5/2010 Aubel et al.
2010/0151652 A1 6/2010 Lung et al.
2010/0163830 A1 7/2010 Chang et al.
2010/0163833 A1 7/2010 Borghi et al.
2010/0165719 A1 7/2010 Pellizzer
2010/0176368 A1 7/2010 Ko et al.
2010/0176911 A1 7/2010 Park et al.
2010/0207168 A1 8/2010 Sills et al.
2010/0213431 A1 8/2010 Yeh et al.
2010/0221874 A1 9/2010 Kuo et al.
2010/0270529 A1 10/2010 Lung
2010/0301303 A1 12/2010 Wang et al.
2010/0301304 A1 12/2010 Chen et al.
2010/0301417 A1 12/2010 Cheng et al.
2010/0308296 A1 12/2010 Pirovano et al.
2010/0323490 A1 12/2010 Sreenivasan et al.
2010/0327251 A1 12/2010 Park
2011/0001114 A1 1/2011 Zanderighi et al.
2011/0031461 A1 2/2011 Kang et al.
2011/0068318 A1* 3/2011 Ishibashi H01L 27/101 257/5
2011/0074538 A1 3/2011 Wu et al.
2011/0092041 A1 4/2011 Lai et al.
2011/0155984 A1 6/2011 Redaelli et al.
2011/0193042 A1 8/2011 Maxwell
2011/0193049 A1 8/2011 Iwakaji et al.
2011/0215436 A1 9/2011 Tang et al.
2011/0284815 A1 11/2011 Kim et al.
2011/0300685 A1 12/2011 Horii et al.
2011/0312178 A1 12/2011 Watanabe et al.
2012/0241705 A1 9/2012 Bresolin et al.
2012/0256150 A1 10/2012 Zagrebelny et al.
2012/0256151 A1 10/2012 Liu et al.
2012/0273742 A1 11/2012 Minemura
2013/0099888 A1 4/2013 Redaelli et al.
2013/0126816 A1 5/2013 Tang et al.
2013/0277796 A1 10/2013 Yang et al.
2013/0285002 A1 10/2013 Van Gerpen et al.
2014/0117302 A1 5/2014 Goswami
2014/0217350 A1 8/2014 Liu et al.

FOREIGN PATENT DOCUMENTS

WO WO 2010/073904 7/2010
WO PCT/US2012/063962 3/2013
WO WO 2013/039496 3/2013

(56) **References Cited**

FOREIGN PATENT DOCUMENTS

WO PCT/US2012/063962	5/2014
WO PCT/US2014/011250	5/2014
WO PCT/US2014/011250	8/2015

OTHER PUBLICATIONS

U.S. Appl. No. 14/295,770, filed Jun. 4, 2014, Pellizzer.

Bez; Chalcogenide PCM: a Memory Technology for Next Decade; IEEE, 2009, pp. 5.1.1 .5.1.4.

Czubatyj et al., "Current Reduction in Ovonic Memory Devices", downloaded from www.epocs.org/library/papers/pdC2006/pdf.../Czubatyj.pdf; prior to Nov. 17, 2011.

Fazio, "Future Directions of Non-Volatile Memory in Compute Applications", IEEE, 2009, pp. 27.7.1-727,7.4.

Happ et al., "Novel One-Mask Self-Heating Pillar Phase Change Memory", IEEE, 2006 Symposium on 5 VLSI Technology Digest of Technical Papers; 2 pp.

Lee et al.; Programming Disturbance and Cell Scaling in Phase Change Memory: For up to 16nm based 4F2 Cell; IEEE, 2010 Symposium on VLSI Technology Digest ofTechnical Papers, pp. 199-200.

Raoux et al., Effect of Ion Implantation on Crystallization Properties of Phase Change Materials, presented at E\PCOS201 0 Conference, Sep. 6-7, 2010, Politecnico di Milano, Milan, Italy.

Russo et al.; Modeling of Programming and Read Performance in Phase-Change Memories—Part II: Program Disturb and Mixed-Scaling Approach,. IEEE Transactions on Electron Devices, vol. 55(2), Feb. 2008, pp. 5.15-5.22.

Servalli; A 45nm Generation Phase Change Memory Technology; IEEE 2009; pp. IEDM09-113-IEDM09-116.

Villa et al.; A 45nm 1Gb 1.8V Phase-Change Memory; 2010 IEEE International Solid-State Circuits.Conference; Feb. 9, 2010; pp. 270-271.

* cited by examiner

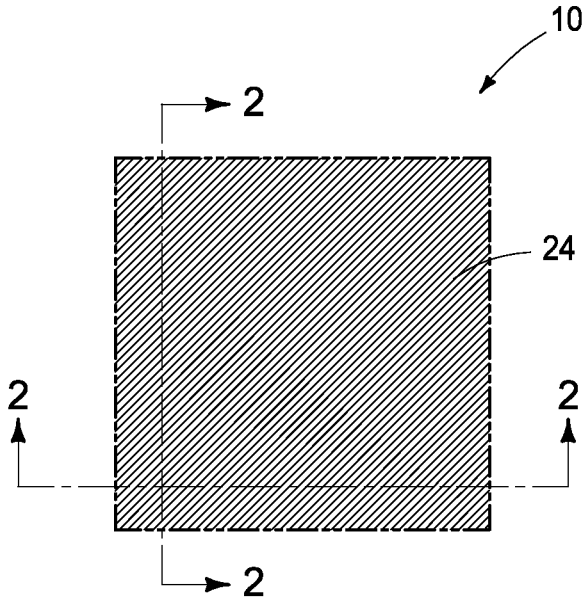


FIG. 1

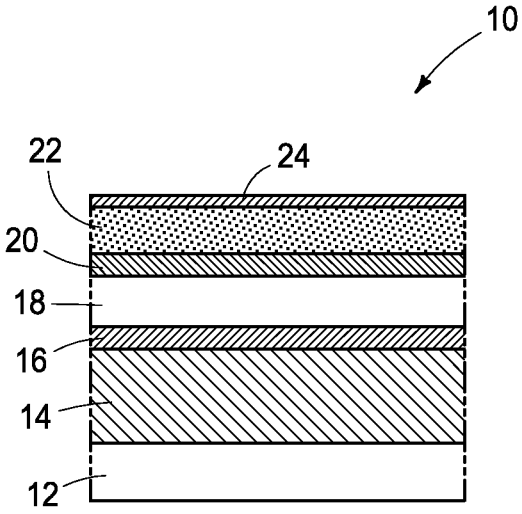


FIG. 2

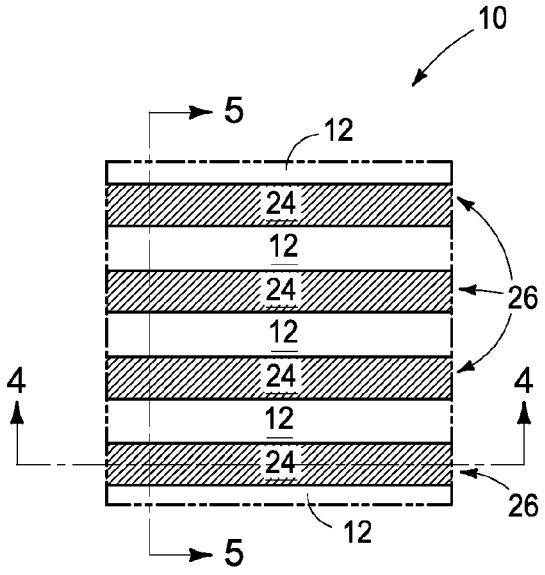


FIG. 3

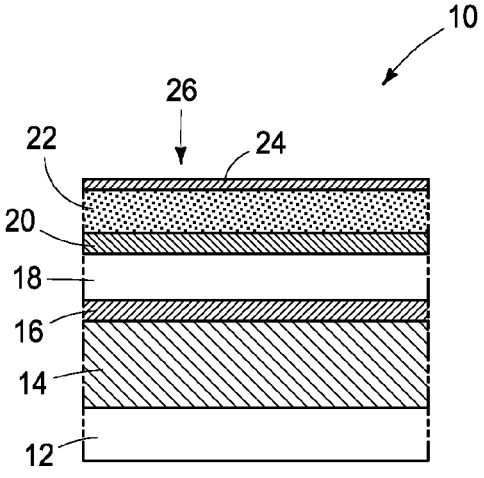


FIG. 4

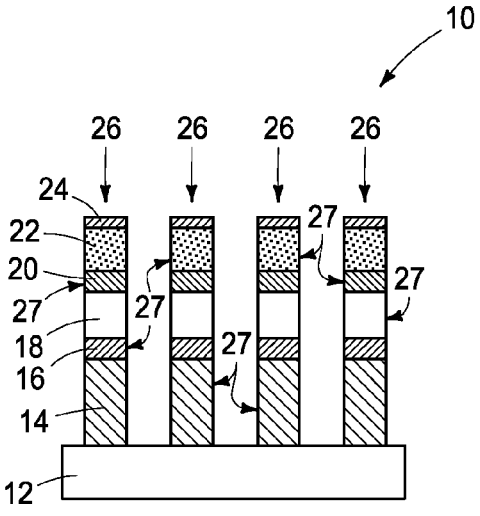


FIG. 5

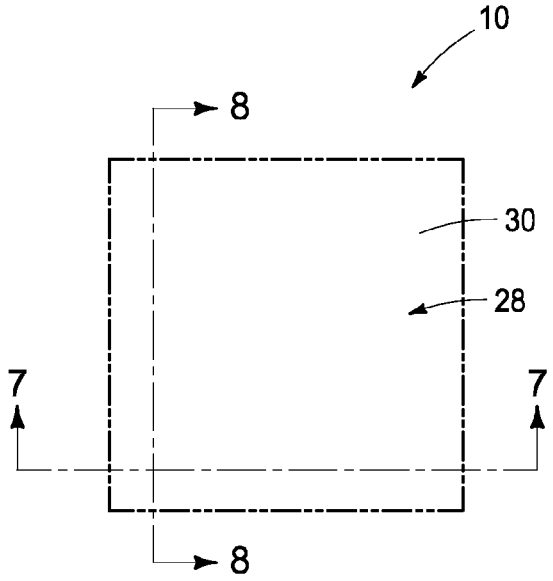


FIG. 6

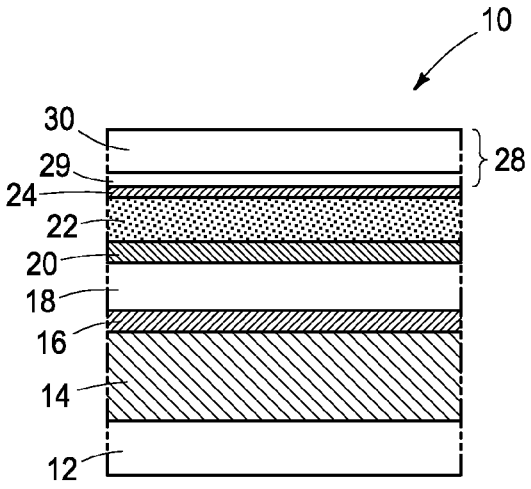


FIG. 7

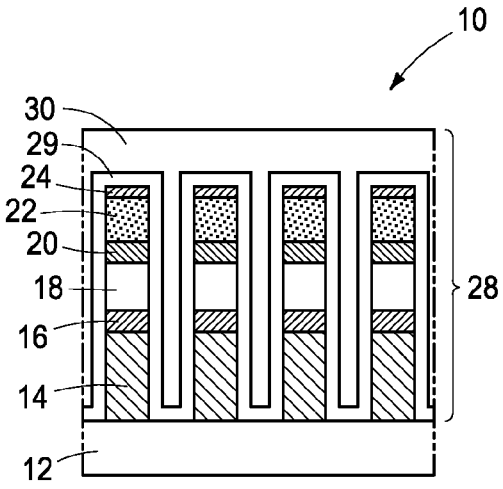


FIG. 8

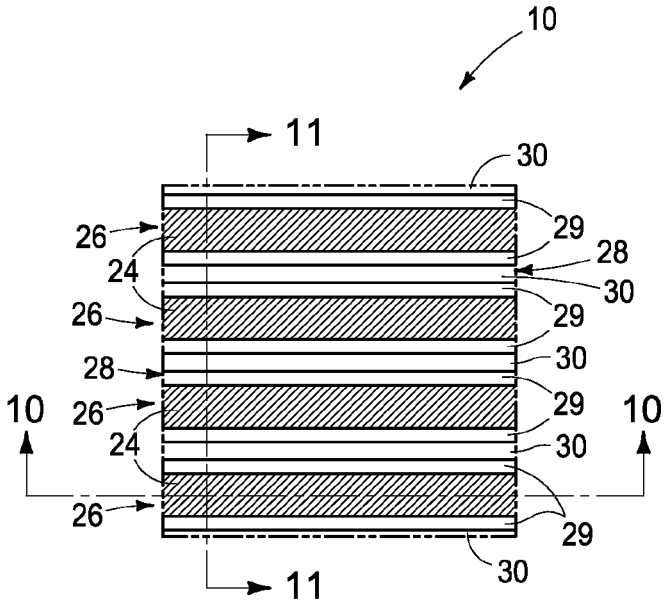


FIG. 9

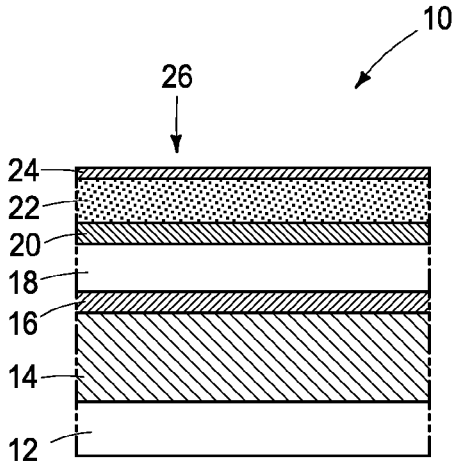


FIG. 10

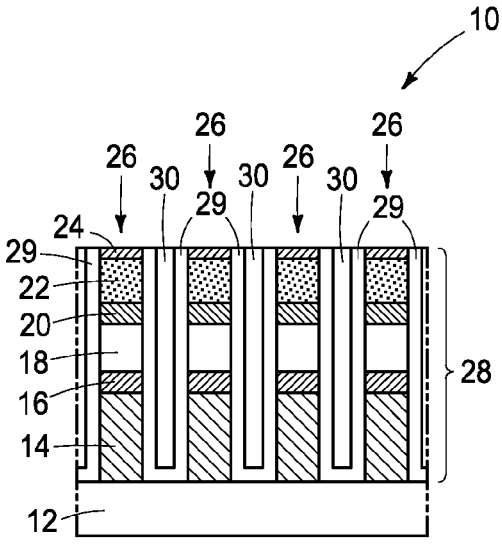


FIG. 11

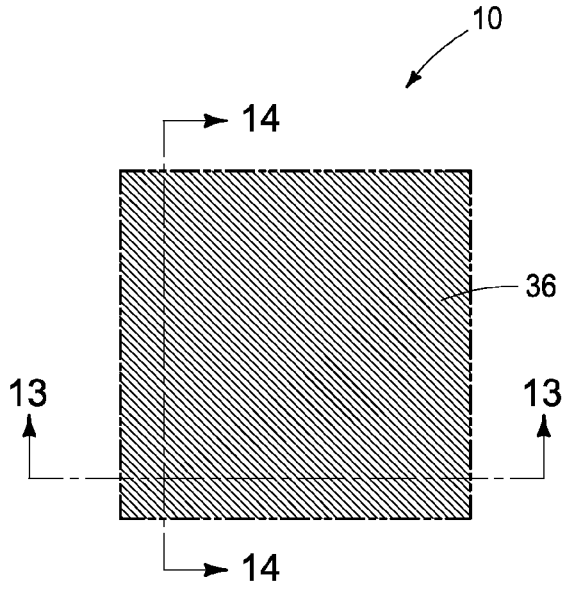


FIG. 12

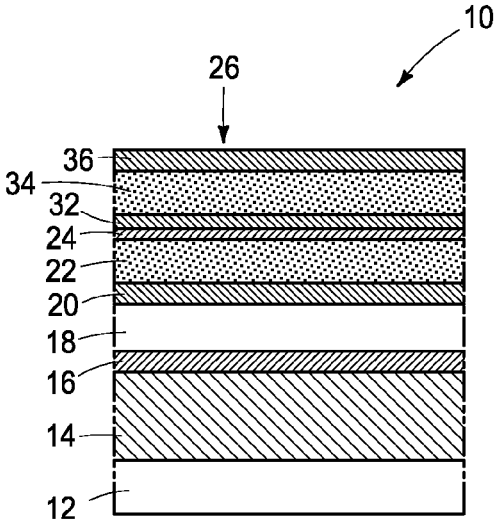


FIG. 13

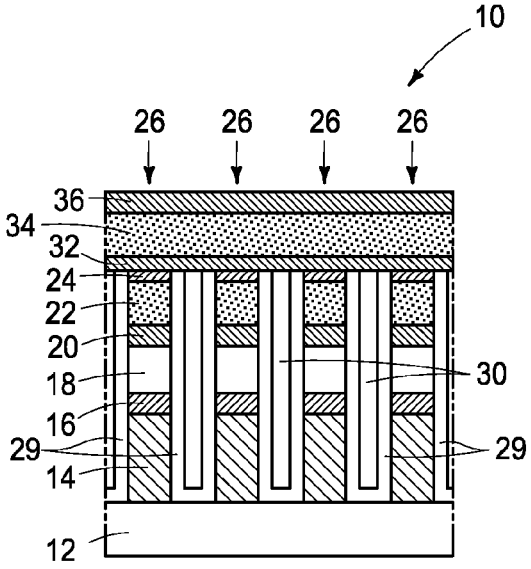


FIG. 14

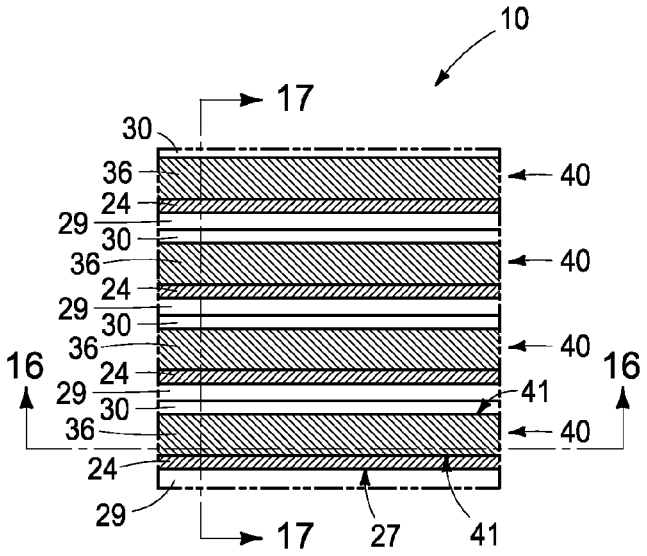


FIG. 15

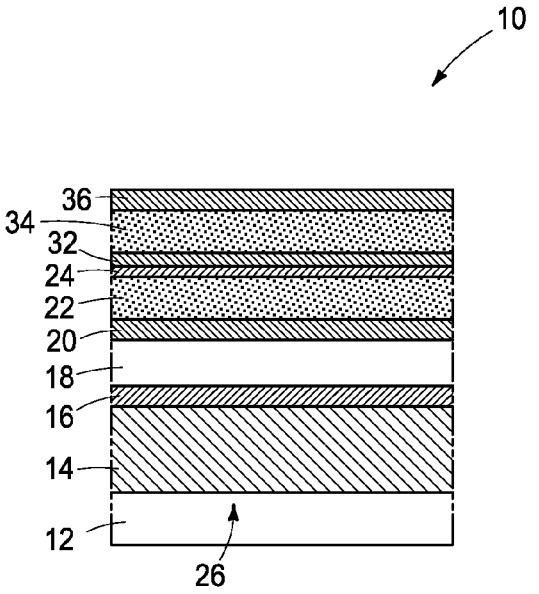


FIG. 16

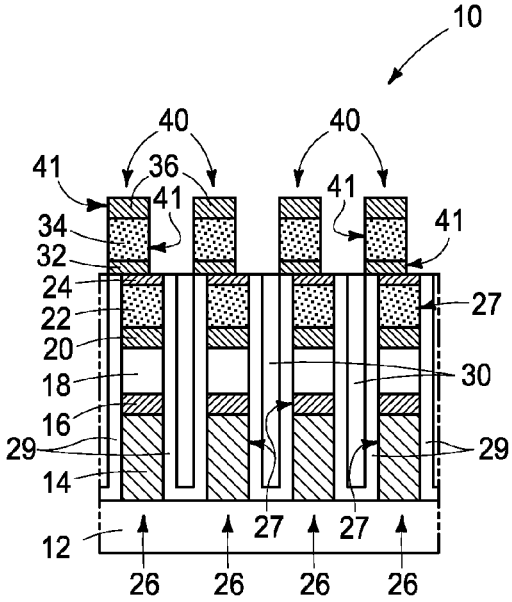


FIG. 17

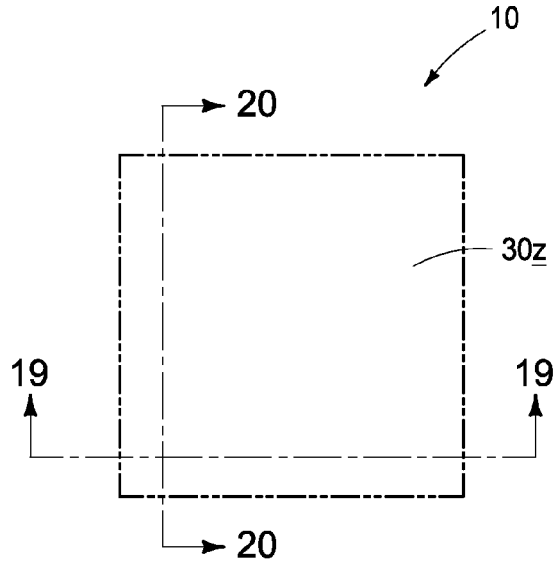


FIG. 18

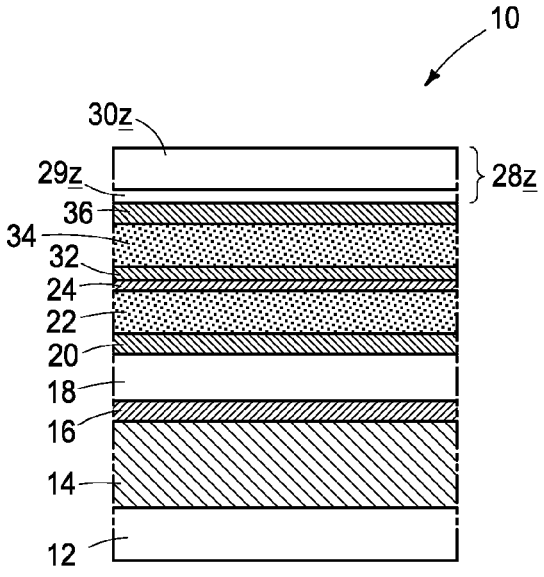


FIG. 19

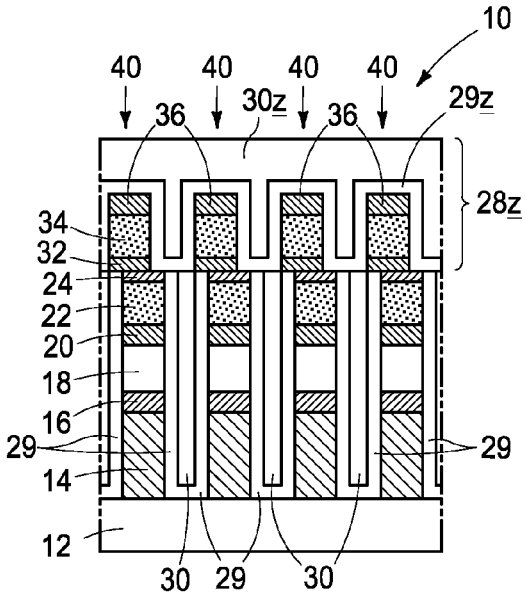


FIG. 20

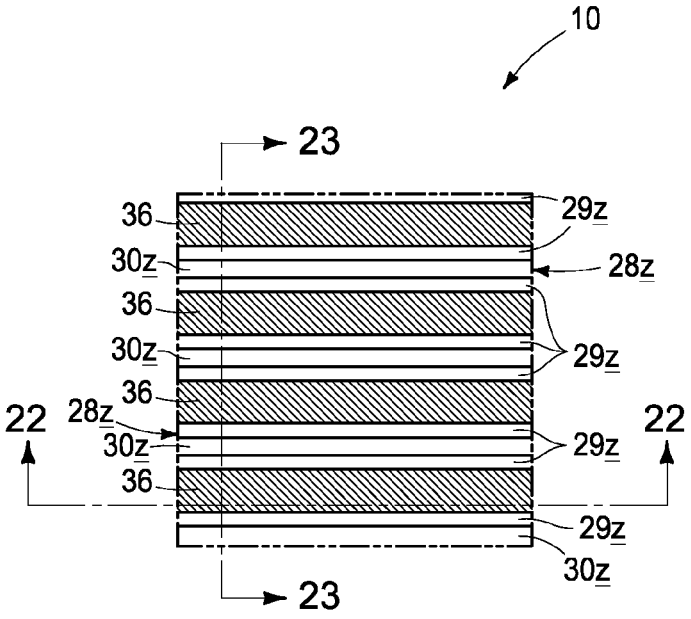


FIG. 21

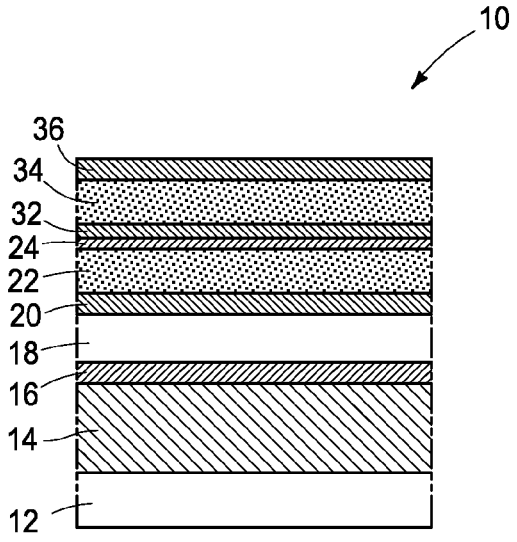


FIG. 22

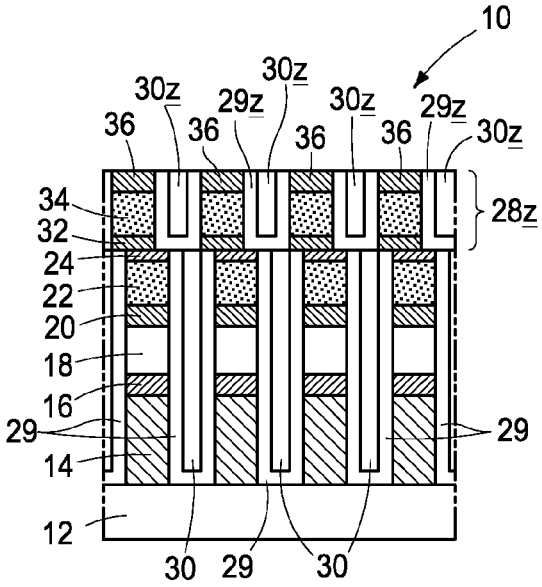


FIG. 23

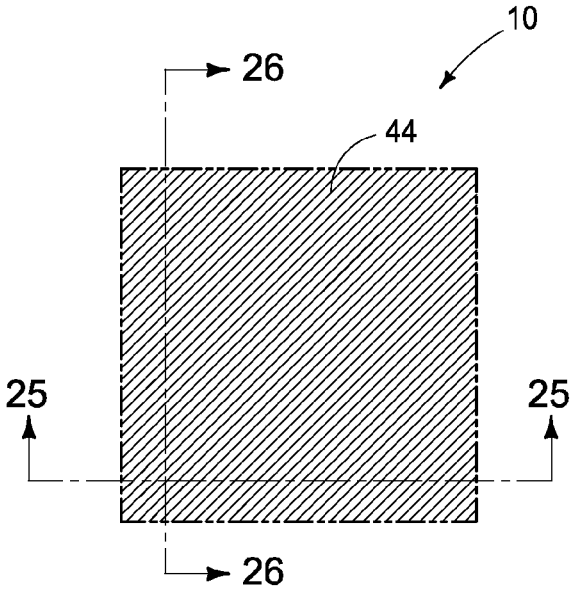


FIG. 24

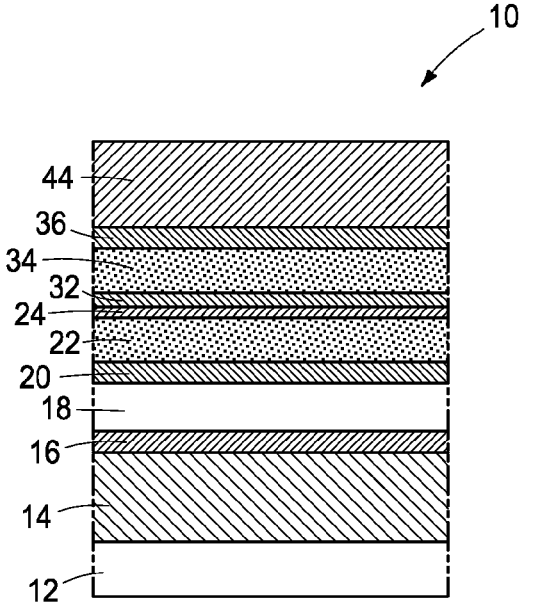


FIG. 25

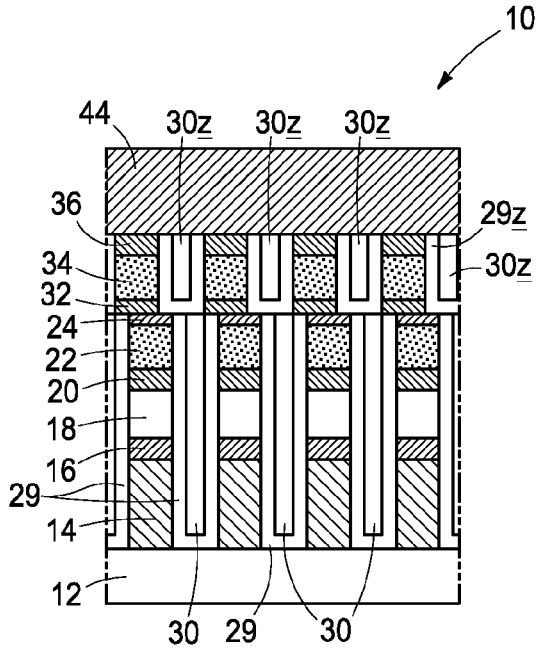


FIG. 26

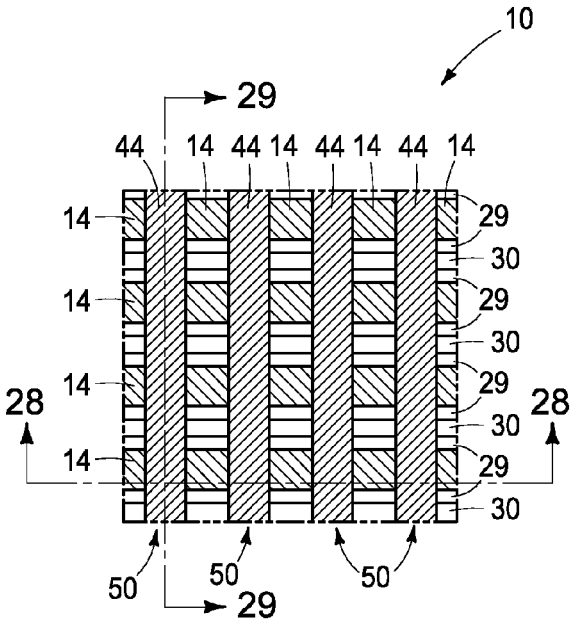


FIG. 27

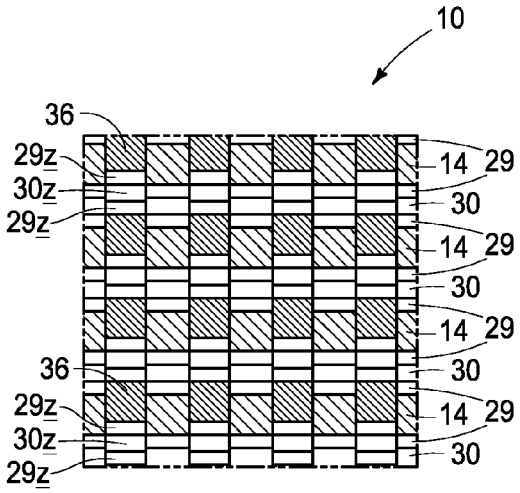


FIG. 30

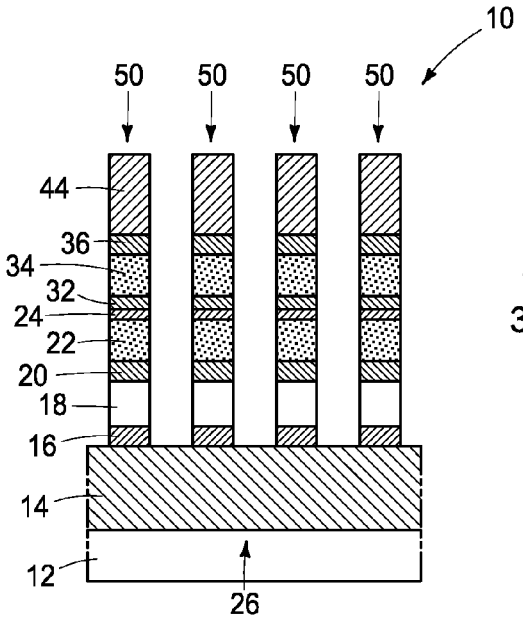


FIG. 28

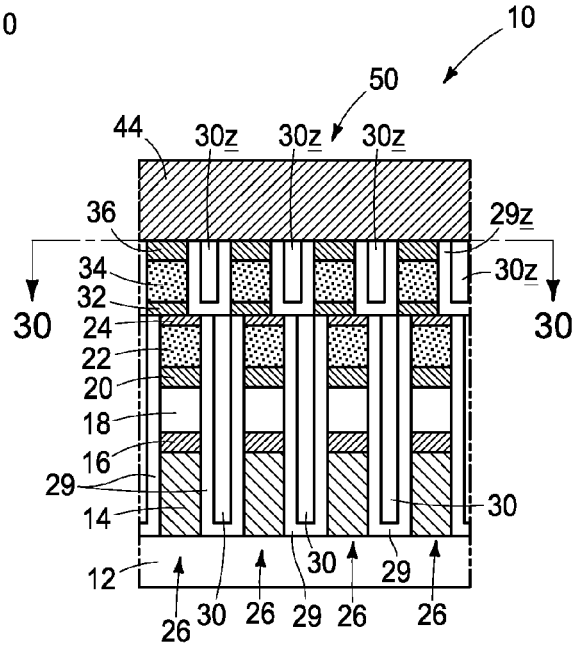


FIG. 29

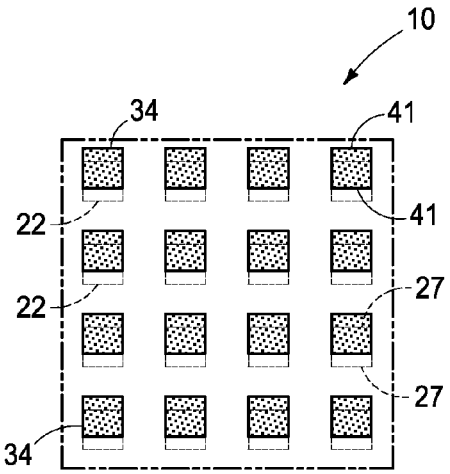


FIG. 31

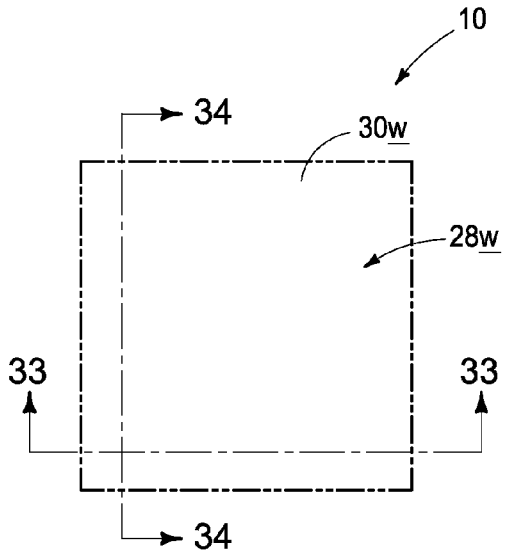


FIG. 32

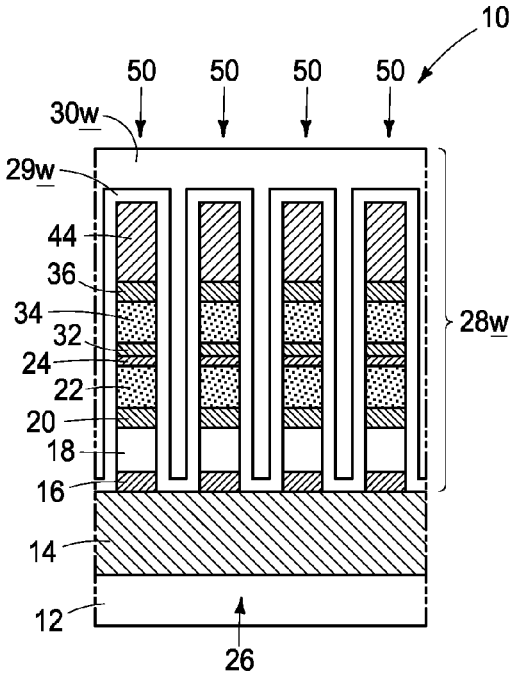


FIG. 33

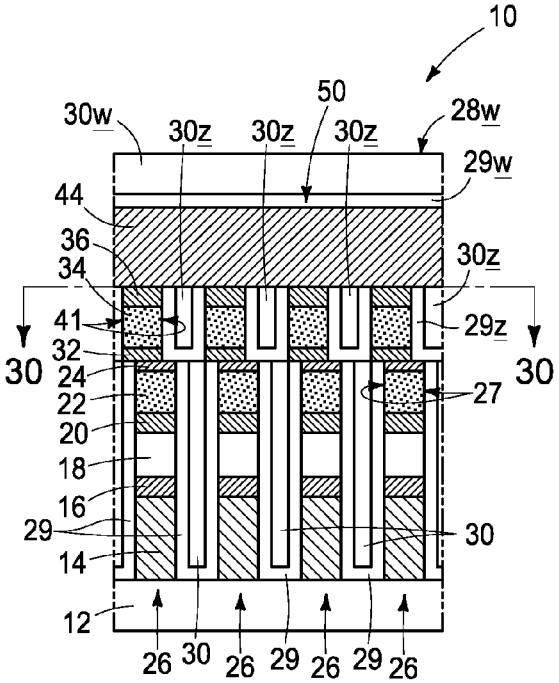


FIG. 34

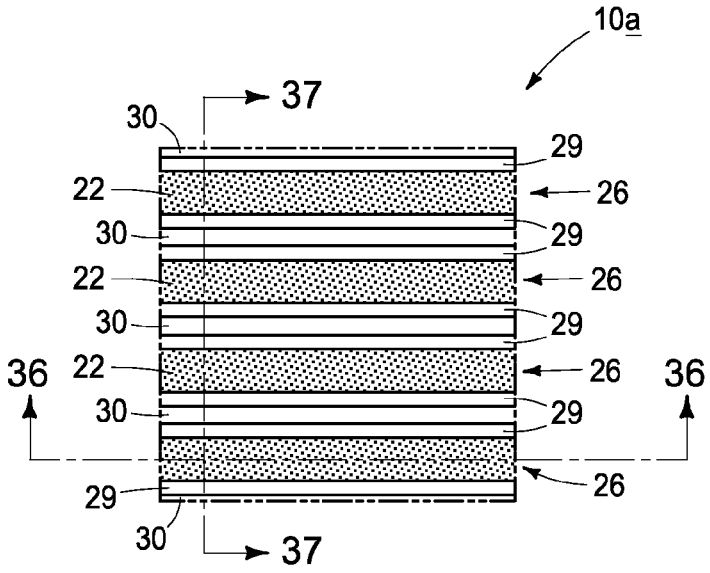


FIG. 35

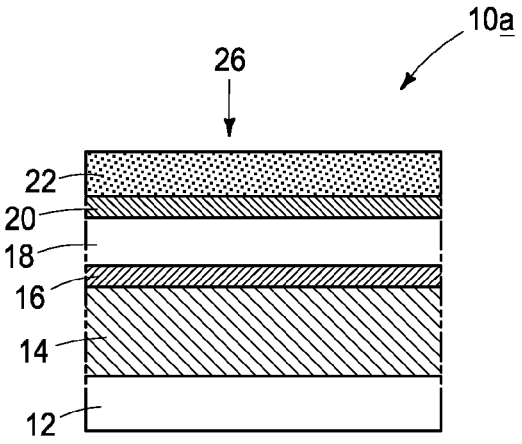


FIG. 36

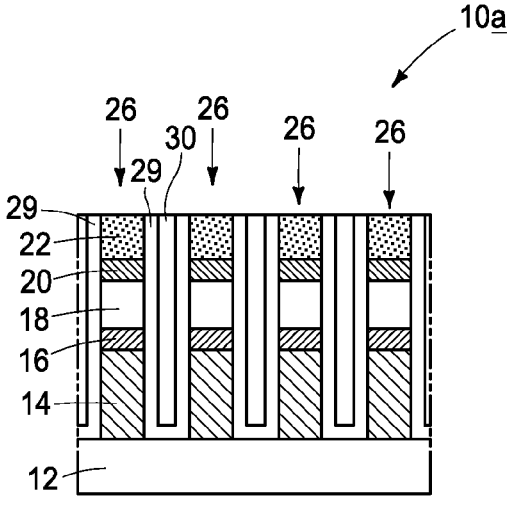


FIG. 37

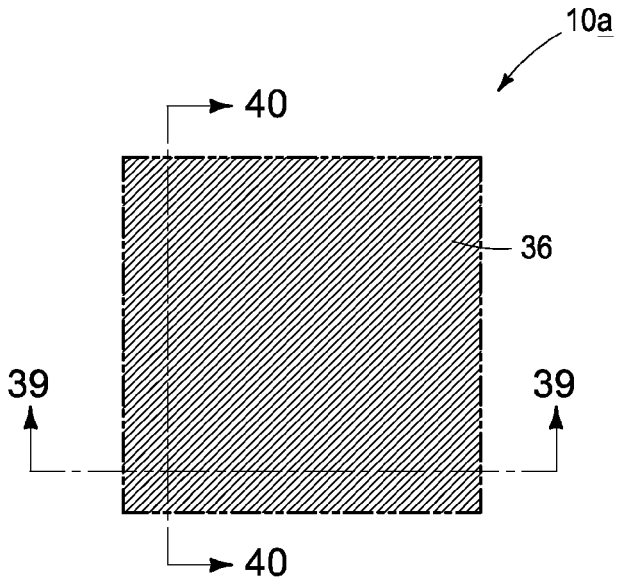


FIG. 38

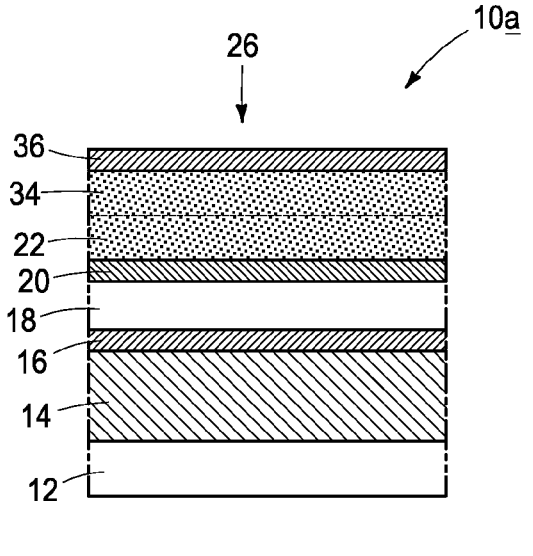


FIG. 39

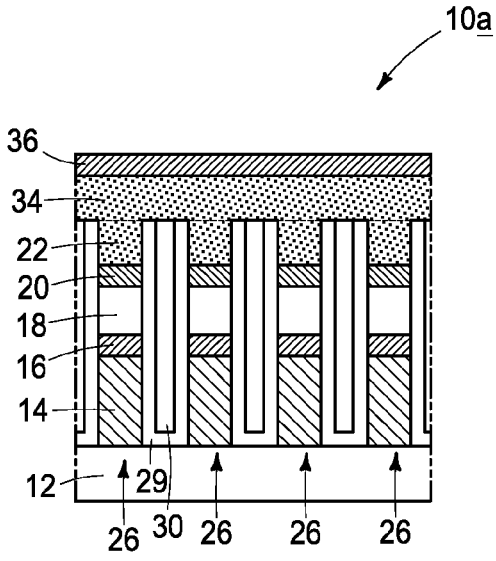


FIG. 40

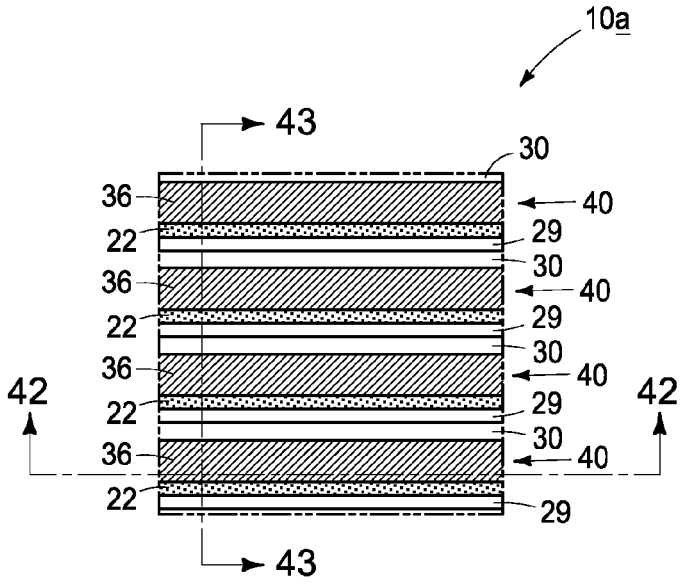


FIG. 41

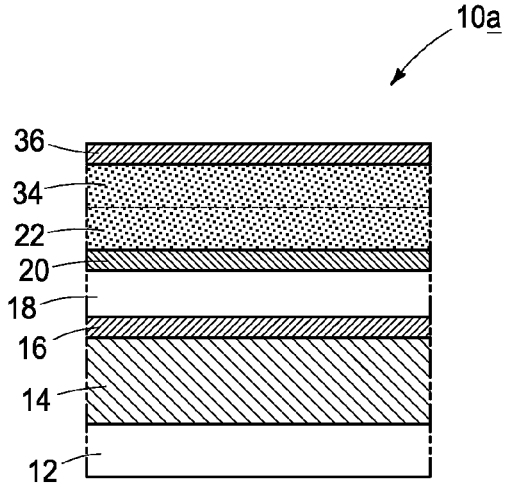


FIG. 42

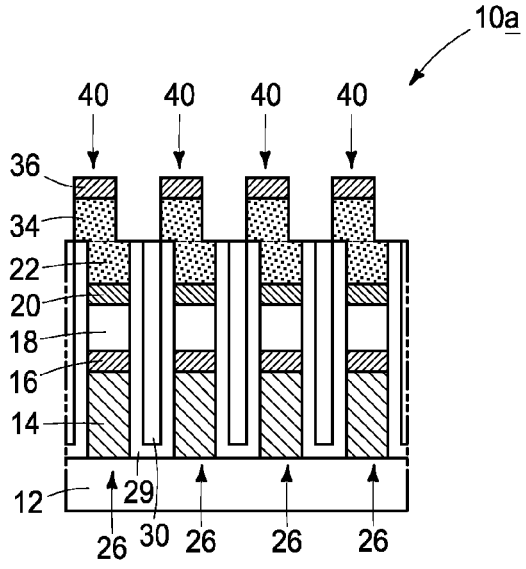


FIG. 43

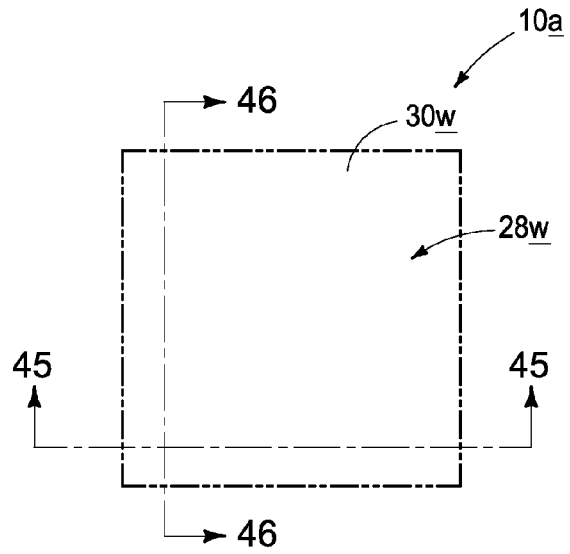


FIG. 44

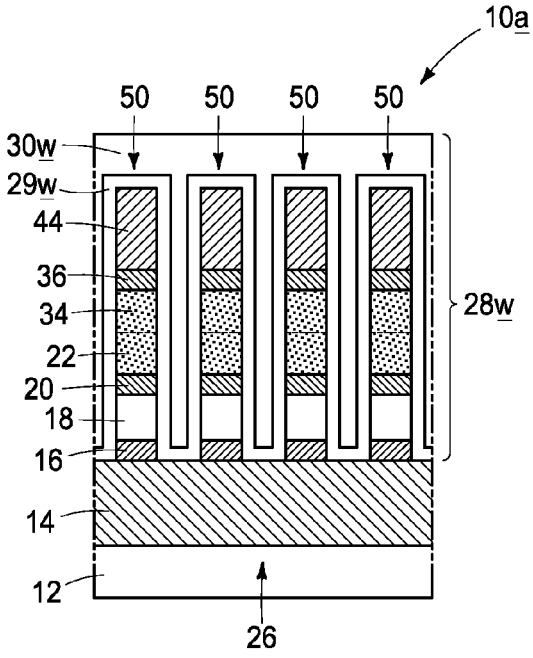


FIG. 45

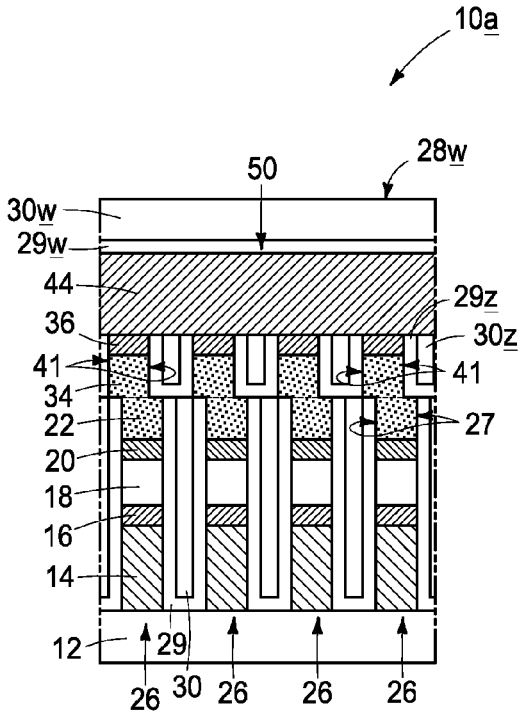


FIG. 46

ARRAY OF CROSS POINT MEMORY CELLS AND METHODS OF FORMING AN ARRAY OF CROSS POINT MEMORY CELLS

TECHNICAL FIELD

Embodiments disclosed herein pertain to arrays of cross point memory cells and to methods of forming arrays of cross point memory cells.

BACKGROUND

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Integrated memory is usually fabricated in one or more arrays of individual memory cells. The memory cells are configured to retain or store memory in at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store more than two levels or states of information. The memory cells might be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time in the absence of power. Nonvolatile memory is conventionally specified to be memory having a retention time of at least about 10 years. Volatile memory dissipates, and is therefore refreshed/rewritten to maintain data storage. Volatile memory may have a retention time of milliseconds, or less.

Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. There is a continuing effort to reduce the number of components in individual devices because such can reduce the size of finished constructions and simplify processing. The smallest and simplest memory cell will likely be comprised of two electrodes having a programmable material, and possibly a select device (such as a diode or ovonic threshold switch), received between them. Suitable programmable materials have two or more selectable memory states to enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a predetermined state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

One type of non-volatile memory is phase change memory. Such memory uses a reversibly programmable material that has the property of switching between two different phases, for example between an amorphous, disorderly phase and a crystalline or polycrystalline, orderly phase. The two phases may be associated with resistivities of significantly different values. Presently, typical phase change materials are chalcogenides, although other materials may be developed. With chalcogenides, the resistivity may vary by two or more orders of magnitude when the material passes between the amorphous (more resistive) phase and the crystalline (more conductive) phase. Phase change can be obtained by locally increasing the temperature of the chalcogenide. Below 150° C., both phases are stable. Starting from an amorphous state and rising to temperature above about 400° C., a rapid nucleation of the crystallites may occur and, if the material is kept at the crystallization temperature for a sufficiently long time, it undergoes a phase change to become crystalline. Reversion to the amorphous state can result by raising the temperature above the melting temperature (about 600° C.) followed by cooling.

In phase change memory, a plurality of memory cells is typically arranged in rows and columns to form an array or sub-array. Each memory cell is coupled to a respective select or access device which may be implemented by any switchable device, such as a PN diode, a bipolar junction transistor, a field effect transistor, etc. The access device is often electrically coupled with, or forms a part of, what is referred to as an access line or word line. A resistive electrode is electrically coupled with the switchable device, and comprises heater material which is configured to heat up upon sufficient current flowing there-through. The phase change material is provided in proximity to the heater material, thereby forming a programmable storage element. The crystallization temperature and the melting temperature are obtained by causing an electric current to flow through the heater material, thus heating the phase change material. Alternately, the access device may be essentially sufficiently self-heating upon current flow there-through whereby separate heater material is not used. Regardless, an electrode, typically referred to as a bit, digit, or select line, is electrically coupled to the phase change material.

Multi-resistive state materials, such as phase change materials, can pose challenges during manufacture. For example in cross point memory, individual memory cells may encompass a multi-resistive state material between a top electrode and a middle electrode. A select device may be between the middle electrode and a bottom electrode. All of these features may be received elevationally between a bottom electrode line and a crossing top electrode line. Materials of all this components should be able to withstand all of the processing during fabrication of each material into a desired finished shape. Unfortunately, many phase change materials exhibit mechanical weakness particularly as their thicknesses increase.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic top plan view of a substrate fragment in process in accordance with an embodiment of the invention.

FIG. **2** is a diagrammatic sectional view taken through either of lines **2-2** in FIG. **1**.

FIG. **3** is a view of the FIG. **1** substrate at a processing step subsequent to that shown by FIG. **1**.

FIG. **4** is a diagrammatic sectional view taken through line **4-4** in FIG. **3**.

FIG. **5** is a diagrammatic sectional view taken through line **5-5** in FIG. **3**.

FIG. **6** is a view of the FIG. **3** substrate at a processing step subsequent to that shown by FIG. **3**.

FIG. **7** is a diagrammatic sectional view taken through line **7-7** in FIG. **6**.

FIG. **8** is a diagrammatic sectional view taken through line **8-8** in FIG. **6**.

FIG. **9** is a view of the FIG. **6** substrate at a processing step subsequent to that shown by FIG. **6**.

FIG. **10** is a diagrammatic sectional view taken through line **10-10** in FIG. **9**.

FIG. **11** is a diagrammatic sectional view taken through line **11-11** in FIG. **9**.

FIG. **12** is a view of the FIG. **9** substrate at a processing step subsequent to that shown by FIG. **9**.

FIG. **13** is a diagrammatic sectional view taken through line **13-13** in FIG. **12**.

FIG. **14** is a diagrammatic sectional view taken through line **14-14** in FIG. **12**.

FIG. **15** is a view of the FIG. **12** substrate at a processing step subsequent to that shown by FIG. **12**.

FIG. **16** is a diagrammatic sectional view taken through line **16-16** in FIG. **15**.

FIG. **17** is a diagrammatic sectional view taken through line **17-17** in FIG. **15**.

FIG. **18** is a view of the FIG. **15** substrate at a processing step subsequent to that shown by FIG. **15**.

FIG. **19** is a diagrammatic sectional view taken through line **19-19** in FIG. **18**.

FIG. **20** is a diagrammatic sectional view taken through line **20-20** in FIG. **18**.

FIG. **21** is a view of the FIG. **18** substrate at a processing step subsequent to that shown by FIG. **18**.

FIG. **22** is a diagrammatic sectional view taken through line **22-22** in FIG. **21**.

FIG. **23** is a diagrammatic sectional view taken through line **23-23** in FIG. **21**.

FIG. **24** is a view of the FIG. **21** substrate at a processing step subsequent to that shown by FIG. **21**.

FIG. **25** is a diagrammatic sectional view taken through line **25-25** in FIG. **24**.

FIG. **26** is a diagrammatic sectional view taken through line **26-26** in FIG. **24**.

FIG. **27** is a view of the FIG. **24** substrate at a processing step subsequent to that shown by FIG. **24**.

FIG. **28** is a diagrammatic sectional view taken through line **28-28** in FIG. **27**.

FIG. **29** is a diagrammatic sectional view taken through line **29-29** in FIG. **27**.

FIG. **30** is a diagrammatic sectional view taken through line **30-30** in FIG. **29**, and is rotated 90° to conform to the substrate positioning as shown in FIG. **27**.

FIG. **31** is a diagrammatic sectional view of the FIG. **28** substrate.

FIG. **32** is a view of the FIG. **28** substrate at a processing step subsequent to that shown by FIG. **28**.

FIG. **33** is a diagrammatic sectional view taken through line **33-33** in FIG. **32**.

FIG. **34** is a diagrammatic sectional view taken through line **34-34** in FIG. **32**.

FIG. **35** is a diagrammatic top plan view of a substrate fragment in process in accordance with an embodiment of the invention.

FIG. **36** is a diagrammatic sectional view taken through line **36-36** in FIG. **35**.

FIG. **37** is a diagrammatic sectional view taken through line **37-37** in FIG. **35**.

FIG. **38** is a view of the FIG. **35** substrate at a processing step subsequent to that shown by FIG. **35**.

FIG. **39** is a diagrammatic sectional view taken through line **39-39** in FIG. **38**.

FIG. **40** is a diagrammatic sectional view taken through line **40-40** in FIG. **38**.

FIG. **41** is a view of the FIG. **38** substrate at a processing step subsequent to that shown by FIG. **38**.

FIG. **42** is a diagrammatic sectional view taken through line **42-42** in FIG. **41**.

FIG. **43** is a diagrammatic sectional view taken through line **43-43** in FIG. **41**.

FIG. **44** is a view of the FIG. **41** substrate at a processing step subsequent to that shown by FIG. **41**.

FIG. **45** is a diagrammatic sectional view taken through line **45-45** in FIG. **44**.

FIG. **46** is a diagrammatic sectional view taken through line **46-46** in FIG. **44**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example methods of forming an array of cross point memory cells are initially described with referring to FIGS. **1-34**. FIGS. **1** and **2** show a substrate fragment **10** comprising a base substrate **12** having various materials formed thereover. Substrate **12** may comprise a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Partially or wholly fabricated components of integrated circuitry may be formed as part of, or be elevationally inward of, substrate material **12**.

Any of the materials and/or structures described herein may be homogenous or non-homogenous, and regardless may be continuous or discontinuous over any material that such overlie. As used herein, "different composition" only requires those portions of two stated materials that may be directly against one another to be chemically and/or physically different, for example if such materials are not homogenous. If the two stated materials are not directly against one another, "different composition" only requires that those portions of the two stated materials that are closest to one another be chemically and/or physically different if such materials are not homogenous. In this document, a material or structure is "directly against" another when there is at least some physical touching contact of the stated materials or structures relative one another. In contrast, "over", "on", and "against" not preceded by "directly", encompass "directly against" as well as construction where intervening material(s) or structure(s) result(s) in no physical touching contact of the stated materials or structures relative one another. Further, unless otherwise stated, each material may be formed using any suitable existing or yet-to-be-developed technique, with atomic layer deposition, chemical vapor deposition, physical vapor deposition, epitaxial growth, diffusion doping, and ion implanting being examples.

Inner conductive (i.e., electrically) electrode material **14** has been formed over base substrate **12**. Example compositions for electrode material **14** are elemental metals, a mixture or alloy of two or more elemental metals, conductive metal compounds, and conductively-doped semiconductive materials. An example thickness for material **14** is about 20 to 100 nm. In this document, "thickness" by itself (no preceding directional adjective) is defined as the mean straight-line distance through a given material or region perpendicularly from a closest surface of an immediately adjacent material of different composition or of an immediately adjacent region. Additionally, the various materials described herein may be of substantially constant thickness or of variable thicknesses. If of variable thickness, thickness refers to average thickness.

Conductive bottom electrode material **16** has been formed over inner electrode material **14**, and in one embodiment directly against material **14**. In this document, "elevational", "upper", "lower", "top", and "bottom" are with reference to the vertical direction. "Horizontal" refers to a general direction along a primary surface relative to which the substrate is processed during fabrication, and vertical is a direction generally orthogonal thereto. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative

one another independent of orientation of the substrate in three-dimensional space. An example thickness for bottom electrode material **16** is about 10 to 50 nm. Example compositions are as described above for material **14**.

Select device material **18** has been formed over bottom electrode material **16**, and in one embodiment directly against material **16**. Such may be formed of any suitable material(s) to provide a select device function (e.g., as a diode or ovonic threshold switch). An example thickness for select device material **18** is about 10 to 40 nm. Conductive mid-electrode material **20** has been formed over select device material **18**, and in one embodiment directly against material **18**. Example compositions for mid-electrode material **20** are as described above for material **16**. Additionally or alternately, material **16** may comprise heater material particularly when multi-resistive state material described below comprises phase change material and where programming occurs by heating. Example heater materials are TiSiN-based materials and TiN-based materials having material other than silicon therein. An example thickness for mid-electrode material **20** is about 5 to 50 nm. Bottom electrode material **16** and/or mid-electrode material **20** may have diffusion barrier properties. Bottom electrode material **16** may also comprise heater material.

Inner multi-resistive state material **22** is formed elevationally over mid-electrode material **20**, and in one embodiment directly against material **20**. In one embodiment, such comprises phase change material, with example compositions being chalcogenides such as GeSbTe-based materials. Other multi-resistive state materials may be used, such as multi-resistive state metal oxide-comprising materials, for example comprising two different layers or regions generally regarded as or understood to be active or passive regions, although not necessarily. Example active cell region compositions which comprise metal oxide and can be configured in multi-resistive states include one or a combination of $Sr_xRu_yO_z$, Ru_xO_y, and $In_xSn_yO_z$. Other examples include MgO, Ta_2O_5, $SrTiO_3$, ZrO_x (perhaps doped with La), and $CaMnO_3$ (doped with one or more of Pr, La, Sr, or Sm). Example passive cell region compositions include one or a combination of Al_2O_3, TiO_2, and HfO_2. Regardless, an example thickness for inner multi-resistive state material **22** is about 10 to 30 nm.

Material **24** is formed elevationally over inner multi-resistive state material **22**, and in one embodiment directly against material **22**. In one embodiment, material **24** is at least one of metal material and semi-metal material. In this document, a "metal material" contains metal in any of elemental, alloy, and compound forms and has an electrical resistance of less than 1×10^{-4} ohm·cm. Examples are elemental metals, a mixture or alloy of two or more elemental metals, and conductive metal compounds, such as tungsten, tungsten nitride, titanium, and titanium nitride. In this document, a "semi-metal material" is any composition having an electrical resistance of from 1×10^{-4} ohm·cm to 1×10^{-2} ohm·cm. Examples include titanium-silicon-nitride (e.g., heater material), conductively doped semiconductive materials, and tungsten carbide. In one embodiment, material **24** is not programmable material (i.e., it is intrinsically not capable of being programmed to different resistive states). An example thickness for material **24** is about 2 to 20 nm.

Referring to FIGS. **3-5**, materials **14-24** have been patterned to form spaced first lines **26**. An example technique includes photolithographic patterning and etch. Regardless, pitch multiplication may be used. First lines **26** may be considered as having longitudinal edges **27**.

Referring to FIGS. **6-8**, dielectric material **28** has been deposited to cover over material **24**, in one embodiment directly against material **24**, and to overfill spaces between first lines **26**. In one embodiment and as shown, dielectric material **28** comprises a first dielectric material **29** (e.g., silicon nitride) and a second dielectric material **30** (e.g., doped or undoped silicon dioxide). Two different composition dielectric materials **29**, **30** may be used where a more desired dielectric material **30** would otherwise react or negatively interact with one of more of materials **14-24**.

Referring to FIGS. **9-11**, dielectric material **28** has been polished back to expose material **24**, and in one embodiment using material **24** as a polish stop. Example polishing techniques include mechanical polishing and chemical mechanical polishing.

Referring to FIGS. **12-14**, and in one embodiment, material **24** may be considered as lower material that is formed prior to forming first lines **26**. Upper material **32** is formed over, and in one embodiment directly against, lower material **24**. Upper material **32** comprises at least one of metal material and semi-metal material. Examples include those materials described above for material **24**. Lower material **24** and upper material **32** may be of the same composition or of different compositions relative one another. An example thickness for upper material **32** is about 2 to 20 nm.

Outer multi-resistive state material **34** is formed elevationally over upper material **32**, and in one embodiment directly against material **32**. Example outer multi-resistive state materials are the same as those described above for inner multi-resistive state material **22**. Materials **22** and **34** may be of the same composition or of different compositions relative one another, and/or of same or different thickness relative one another. An example thickness for outer multi-resistive state material **34** is about 10 to 30 nm. In the depicted embodiment, outer multi-resistive state material **34** electrically couples to inner multi-resistive state material **22** through materials **32** and **24** (e.g., a contact resistance between materials **34** and **22** of no greater than about 10^{-7} ohm·cm^2 when materials **34** and **22** are programmed to be in a respective highest conductivity state). In one embodiment, one or both of materials **32** and **24** are formed to be intrinsically of higher conductivity (i.e., electrical) than each of inner multi-resistive state material **22** and outer multi-resistive state material **34** when materials **22** and **34** are programmed to be in a respective highest conductivity state. FIGS. **12-14** depict an example embodiment wherein outer multi-resistive state material **34** is not formed directly against inner multi-resistive state material **22** within the array. Alternate embodiments are described below, and which may or may not include use of one or both of materials **24** and **32**.

Conductive top electrode material **36** is formed over outer multi-resistive state material **34**, and in one embodiment directly against material **34**. Example materials include any of those described above for material **16**. An example thickness for material **36** is about 10 to 50 nm. Top electrode material **36**, upper material **32**, and/or lower material **24** may have diffusion barrier properties.

Referring to FIGS. **15-17**, materials **32**, **34**, and **36** have been patterned to form spaced second lines **40** that individually are elevationally over, longitudinally along, and electrically coupled to inner multi-resistive state material **22** of first lines **26**. In one embodiment, second lines **40** are formed to have longitudinal edges **41** that are laterally offset from longitudinal edges **27** of first lines **26**. Such may result as an artifact of manufacture where, for example, a mask pattern for second lines **40** is the same as a mask pattern for first lines **26** and mis-alignment occurs of those masks relative to one another. Alternately, a lateral offset may be intentional. Regardless, such will result in less contact area between multi-resistive state materials **22**, **34** than would occur if

perfect alignment was achieved of the mask for forming second lines **40** relative to that for forming first lines **26**. Forming at least upper material **32** to be of higher conductivity than material **34** when in its highest conductivity state may facilitate reduction of contact resistance between materials **22** and **34**.

Referring to FIGS. **18-20**, dielectric material **28***z* has been deposited to cover over top electrode material **36** and overfill spaces between second lines **40**. Material **28***z* may comprise first and second dielectric material **29***z* and **30***z*, respectively, with example compositions being those as described above for dielectric materials **29** and **30**, respectively.

Referring to FIGS. **21-23**, dielectric material **28***z* has been polished back to expose top electrode material **36**.

Referring to FIGS. **24-26**, outer conductive material **44** has been formed elevationally over top electrode material **36**, and in one embodiment directly against material **36**. Outer conductive material **44** in the depicted embodiment electrically couples to patterned outer multi-resistive state material **34** through top electrode material **36**. Example compositions and thickness for outer conductive material are the same as those described above for inner electrode material **14**.

Referring to FIGS. **27-30**, materials **16**, **18**, **20**, **22**, **24**, **32**, **34**, **36**, **44**, **29**, **30**, **29***z*, and **30***z* have been patterned to form spaced third lines **50** which comprise outer conductive material **44** crossing elevationally over and electrically coupled to previously-patterned (e.g., partially patterned) outer multi-resistive state material **34**. Example techniques for forming lines **50** include photolithographic patterning and etch. Regardless, pitch multiplication may be used. In one embodiment, the forming of third lines **50** within the array comprises etching using a mask (the mask not being shown). The etching using the mask in such embodiment may comprise etching top electrode material **36**, inner and outer multi-resistive state materials **34**, **22**, and bottom electrode material **16** (i.e., at least these materials) inwardly to inner conductive electrode material **14**.

Lines **50** comprise continuously-running outer conductive material **44** and remaining lines **26** comprise continuously-running inner conductive material **14**. Lines **26** may be considered and/or function as access row lines. Lines **50** may be considered and/or function as sense column lines. However, use of "row" and "column" in this document is for convenience in distinguishing one series of lines from another series of lines. Accordingly, "row" and "column" are intended to be synonymous with any series of lines independent of function. Regardless, the rows may be straight and/or curved and/or parallel and/or not parallel relative one another, as may be the columns. Further, the rows and columns may intersect relative one another at 90° or at one or more other angles. In the depicted example, each of the row lines and column lines are shown as being individually straight and angling relative one another at 90°.

FIG. **31** is a diagrammatic depiction showing and comparing horizontal shape and position of outer multi-resistive state material **34** and inner multi-resistive state material **22** relative one another. All other material is not shown for clarity. Materials **36** and **32** may be of the same horizontal shape and position as outer multi-resistive state material **34**. Materials **24**, **20**, **18** and **16** may be of the same horizontal shape and position as inner multi-resistive state material **22**.

Referring to FIGS. **32-34**, dielectric material **28***w* has been deposited to overlie third lines **50** and fill void space between third lines **50** and patterned materials **44**, **36**, **34**, **32**, **24**, **22**, **20**, **18**, and **16**. Material **28***w* may comprise first and second dielectric material **29***w* and **30***w*, respectively, with example compositions being those as described above for dielectric materials **29** and **30**, respectively.

Some embodiments of the invention include a method of forming an array of cross point memory cells comprising patterning inner multi-resistive state material (e.g., material **22**) and inner electrode material (e.g., material **14**) to form spaced first lines (e.g., lines **26**) individually comprising the inner multi-resistive state material elevationally over the electrode material independent of whether other material is present (e.g., regardless of presence of one or more of materials **24**, **20**, **18**, and **16**). Elevationally outer multi-resistive state material (e.g., material **34**) is formed elevationally over and electrically coupled to inner multi-resistive state material (e.g., material **22**) of the first lines independent of whether other material is present (e.g., regardless of presence of one or more of materials **24**, **32**, **28**, **29** and **30**). The outer multi-resistive state material is patterned to form spaced second lines (e.g., lines **40**) that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines. Spaced third lines (e.g., lines **50**) are formed which comprise outer conductive electrode material (e.g., material **44**) crossing elevationally over and electrically coupled to the previously-patterned outer multi-resistive state material independent of whether other material is present (e.g., regardless of presence of one or more of materials **36**, **28**, **29**, **30**, **28***z*, **29***z*, and **30***z*).

Embodiments of the invention encompass using both of lower material **24** and upper material **32**, using neither of lower material **24** and upper material **32**, using only lower material **24** and not using upper material **32**, and using only upper material **32** and not using lower material **24**. When both materials are used and polishing is used before forming the outer multi-resistive state material, composition of lower material **24** may be optimized for use as a polish stop and composition of upper material **32** may be optimized for conductivity (e.g., independent of whether lower material is in the finished circuitry construction).

Additional example embodiments are next described with reference to FIGS. **35-46** with respect to a substrate fragment **10***a*. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. FIGS. **35-37** show a processing sequence corresponding to that of FIGS. **9-11** having occurred relative to a structure as shown in FIGS. **9-11**. However, lower material **24** (not shown in FIGS. **35-37**) may or may not have previously been used. If used, FIGS. **35-37** depict removal having occurred of all remaining of lower material **24** (not shown) from the array after the patterning to form first lines **26**.

Referring to FIGS. **38-40**, outer multi-resistive state material **34** has been formed directly against inner multi-resistive state material **22** (e.g., no upper material **32** has been used). Accordingly, in one embodiment, such shows forming of the outer multi-resistive state material **34** directly against inner multi-resistive state material **22** of individual of first lines **26**.

Referring to FIGS. **41-43**, spaced second lines **40** have been formed analogously to the processing depicted by FIGS. **15-17**. Subsequent processing analogous to that disclosed in FIGS. **18-34** may occur whereby a construction as shown in FIGS. **44-46** results. Any other attribute(s) or construction(s) as described above may be used.

In one embodiment, sacrificial material is formed elevationally over the inner multi-resistive state material. The sacrificial material, the inner multi-resistive state material, and the inner electrode material are patterned to form the spaced first lines individually to comprise the sacrificial material, the

inner multi-resistive state material, and the inner electrode material. All of the sacrificial material is removed before forming the elevationally outer multi-resistive state material. As one example, material **24** may be such sacrificial material. The sacrificial material in this embodiment may be any of metal material, semi-metal material, semiconductive, dielectric, ferroelectric etc. as its electrical properties are not relevant since it is all removed from being part of the spaced first lines.

Embodiments of the invention encompass an array of cross point memory cells independent of method of manufacture. Such an array comprises spaced elevationally inner first lines (e.g., row lines **26**), spaced elevationally outer second lines (e.g., column lines **50**) which cross the first lines, and a multi-resistive state region elevationally between the first and second lines where such cross. Individual of the multi-resistive state regions comprise elevationally outer multi-resistive state material (e.g., material **34**) and inner multi-resistive state material (e.g., material **22**) that are electrically coupled to one another. The inner and outer multi-resistive state materials may be of the same composition relative one another or of different compositions relative one another. Regardless, the inner and outer multi-resistive state materials may be directly against one another or may not be directly against one another.

The inner multi-resistive state material has opposing edges in a vertical cross section, for example opposing edges **27** shown in the vertical cross-sections depicted by FIGS. **34** and **46**. The outer multi-resistive state material has opposing edges in the vertical cross-section that are laterally offset relative to the opposing edges of the inner multi-resistive state material in the vertical cross-section. Such is shown by way of example with respect to opposing edges **41** being offset relative to opposing edges **27** in each of embodiments of FIGS. **34** and **46**. Individual of the memory cells may comprise a select device, for example encompassed by select device material **18** in FIGS. **34** and **46**.

At least one of metal material and semi-metal material may be elevationally between the inner and outer multi-resistive state materials. In one embodiment where present, the at least one of metal material and semi-metal material may be intrinsically of higher conductivity than each of the inner and outer multi-resistive state materials when each is programmed to its highest conductivity state. Regardless, in one embodiment the array may include lower material and upper material, with each comprising at least one of metal material and semi-metal material elevationally between the inner and outer multi-resistive state materials, and with the lower and upper materials being of different compositions relative one another. In one embodiment, the outer multi-resistive state material is directly against the upper material, and the upper material is intrinsically of higher conductivity than each of the inner and outer multi-resistive state materials when each is programmed to its highest conductivity state.

Any other attribute(s) or construction(s) as described above with respect to method may be used in an array of cross point memory cells.

CONCLUSION

In some embodiments, a method of forming an array of cross point memory cells comprises forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material. The inner multi-resistive state material and the inner electrode material are patterned to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner electrode material. Elevationally outer multi-resistive state material is formed elevationally over and electrically coupled to the inner multi-resistive state material of the first lines. The outer multi-resistive state material is patterned to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines. Spaced third lines comprising outer conductive electrode material are formed to cross elevationally over and electrically couple to the patterned outer multi-resistive state material.

In some embodiments, an array of cross point memory cells comprises spaced elevationally inner first lines, spaced elevationally outer second lines which cross the first lines, and a multi-resistive state region elevationally between the first and second lines where such cross. Individual of the multi-resistive state regions comprise elevationally outer multi-resistive state material and elevationally inner multi-resistive state material that are electrically coupled to one another. The inner multi-resistive state material has opposing edges in a vertical cross-section. The outer multi-resistive state material has opposing edges in the vertical cross-section that are laterally offset relative to the opposing edges of the inner multi-resistive state material in the vertical cross-section.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over individual of the first lines, the second lines individually extending longitudinally along and individually being electrically coupled longitudinally along individual of the first lines; and

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material.

2. The method of claim **1** wherein the outer multi-resistive state material is not formed directly against the inner multi-resistive state material within the array.

3. The method of claim **1** comprising forming at least one of metal material and semi-metal material elevationally over the inner multi-resistive state material, the outer multi-resistive state material being formed after forming the at least one of metal material and semi-metal material.

4. The method of claim **3** wherein the at least one comprises metal material.

5. The method of claim 3 wherein the at least one comprises semi-metal material.

6. The method of claim 3 wherein the outer multi-resistive state material is formed elevationally over the at least one of metal material and semi-metal material, and the at least one of metal material and semi-metal material is intrinsically not capable of being programmed to multi-resistive states.

7. The method of claim 3 wherein the at least one of metal material and semi-metal material comprises lower material that is formed prior to the patterning of the inner multi-resistive state material and the inner conductive electrode material to form the first lines, and comprising forming upper material comprising at least one of metal material and semi-metal material directly against the lower material after the patterning of the inner multi-resistive state material and the inner conductive electrode material to form the first lines, the outer multi-resistive state material being formed elevationally over the upper material.

8. The method of claim 7 wherein the outer multi-resistive state material is formed directly against the upper material.

9. The method of claim 8 comprising forming the upper material to be intrinsically of higher conductivity than each of the inner and outer multi-resistive state materials when each is programmed to its highest conductivity state.

10. The method of claim 7 wherein the lower and upper materials are of different compositions.

11. The method of claim 3 comprising, prior to forming the outer multi-resistive state material:

depositing dielectric material to cover over the at least one of metal material and semi-metal material and to overfill spaces between the first lines; and

polishing the dielectric material back to expose the at least one of metal material and semi-metal material using the at least one of metal material and semi-metal material as a polish stop.

12. The method of claim 11 comprising, after the polishing, forming the outer multi-resistive state material to not be directly against the inner multi-resistive state material of individual of the first lines.

13. The method of claim 12 wherein the at least one of metal material and semi-metal material comprises lower material that is formed prior to the patterning of the inner multi-resistive state material and the inner conductive electrode material to form the first lines, and comprising forming upper material comprising at least one of metal material and semi-metal material directly against the lower material after the patterning of the inner multi-resistive state material and the inner conductive electrode material to form the first lines, the outer multi-resistive state material being formed directly against the upper material, and forming the upper material to be intrinsically of higher conductivity than each of the inner and outer multi-resistive state materials when each is programmed to its highest conductivity state.

14. The method of claim 1 comprising:

forming sacrificial material elevationally over the inner multi-resistive state material and patterning the sacrificial material, the inner multi-resistive state material, and the inner conductive electrode material to form said spaced first lines individually to comprise the sacrificial material, the inner multi-resistive state material, and the inner conductive electrode material; and

removing all of the sacrificial material before forming the elevationally outer multi-resistive state material.

15. The method of claim 1 wherein the second lines are formed to have longitudinal edges that are laterally offset from those of the first lines.

16. The method of claim 1 comprising forming select device material over the inner conductive electrode material and forming the inner multi-resistive state material over the select device material.

17. The method of claim 16 comprising forming conductive mid-electrode material over the select device material and forming the inner multi-resistive state material over the conductive mid-electrode material.

18. The method of claim 1 comprising forming conductive bottom electrode material over the inner conductive electrode material and forming the inner multi-resistive state material over the bottom conductive electrode material.

19. The method of claim 18 comprising forming conductive top electrode material over the outer multi-resistive state material and forming the outer conductive electrode material over the conductive top electrode material prior to forming the third lines.

20. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines;

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material; and

the outer multi-resistive state material being formed directly against the inner multi-resistive state material within the array.

21. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines;

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material;

forming at least one of metal material and semi-metal material elevationally over the inner multi-resistive state material, the outer multi-resistive state material being formed after forming the at least one of metal material and semi-metal material; and

sequentially comprising:

after the patterning of the inner multi-resistive state material and the inner conductive electrode material to form the first lines and prior to forming the outer multi-resistive state material, removing all remaining of the at least one of metal material and semi-metal material; and

forming the outer multi-resistive state material directly against the inner multi-resistive state material.

22. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines;

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material;

forming at least one of metal material and semi-metal material elevationally over the inner multi-resistive state material, the outer multi-resistive state material being formed after forming the at least one of metal material and semi-metal material;

prior to forming the outer multi-resistive state material:

depositing dielectric material to cover over the at least one of metal material and semi-metal material and to overfill spaces between the first lines; and

polishing the dielectric material back to expose the at least one of metal material and semi-metal material using the at least one of metal material and semi-metal material as a polish stop; and

after the polishing, forming the outer multi-resistive state material directly against the inner multi-resistive state material of individual of the first lines.

23. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines;

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material; and

wherein forming the third lines within the array comprises etching using a mask, the etching using the mask comprising etching of the outer and inner multi-resistive state materials to form a multi-resistive state region of individual of the memory cells.

24. A method of forming an array of cross point memory cells, comprising:

forming elevationally inner multi-resistive state material elevationally over inner conductive electrode material;

patterning the inner multi-resistive state material and the inner conductive electrode material to form spaced first lines individually comprising the inner multi-resistive state material elevationally over the inner conductive electrode material;

forming elevationally outer multi-resistive state material elevationally over and electrically coupled to the inner multi-resistive state material of the first lines;

patterning the outer multi-resistive state material to form spaced second lines that individually are elevationally over, longitudinally along, and electrically coupled to the inner multi-resistive state material of individual of the first lines;

forming spaced third lines comprising outer conductive electrode material crossing elevationally over and electrically coupled to the patterned outer multi-resistive state material;

forming conductive bottom electrode material over the inner conductive electrode material and forming the inner multi-resistive state material over the bottom conductive electrode material;

forming conductive to electrode material over the outer multi-resistive state material and forming the outer conductive electrode material over the conductive to electrode material prior to forming the third lines; and

wherein forming the third lines within the array comprises etching using a mask; the etching using the mask comprising etching of the conductive top electrode material, the outer and inner multi-resistive state materials, and the bottom conductive electrode material inwardly to the inner conductive electrode material.

* * * * *