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(54) **METHOD AND APPARATUS FOR CALIBRATING AN INPUT INTERFACE**

(56) **References Cited**

(71) Applicant: **Cavium, Inc.**, San Jose, CA (US)

(72) Inventors: **Omer O. Yildirim**, Marlborough, MA (US); **David Lin**, Westborough, MA (US); **Scott E. Meninger**, Groton, MA (US)

(73) Assignee: **Cavium, Inc.**, San Jose, CA (US)

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CPC **H04L 25/06** (2013.01); **H04L 25/028** (2013.01); **H04L 25/0264** (2013.01); **H03M 1/745** (2013.01)

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See application file for complete search history.

U.S. PATENT DOCUMENTS

4,050,030 A	9/1977	Russell	
5,237,533 A	8/1993	Papaliolios	
6,316,992 B1	11/2001	Miao et al.	
6,807,118 B2	10/2004	Perner	
7,576,609 B1	8/2009	Huang et al.	
7,603,084 B2	10/2009	Aytur	
7,755,421 B2*	7/2010	Chen	H03F 3/45973 330/9
7,768,298 B2	8/2010	Park et al.	
7,817,714 B2	10/2010	Bae et al.	
8,391,417 B2	3/2013	Asada et al.	
9,087,567 B2	7/2015	Yildirim et al.	
2006/0274837 A1*	12/2006	Doi	G11C 27/02 375/257
2007/0200619 A1*	8/2007	Jang	H03F 3/45179 330/2
2008/0252504 A1*	10/2008	Jeong	G09G 3/3685 341/144
2010/0315142 A1	12/2010	Zerbe	

(Continued)

OTHER PUBLICATIONS

Non-Final Office Action dated Jun. 19, 2015, Issued in U.S. Appl. No. 14/040,532.

(Continued)

Primary Examiner — Linda Wong

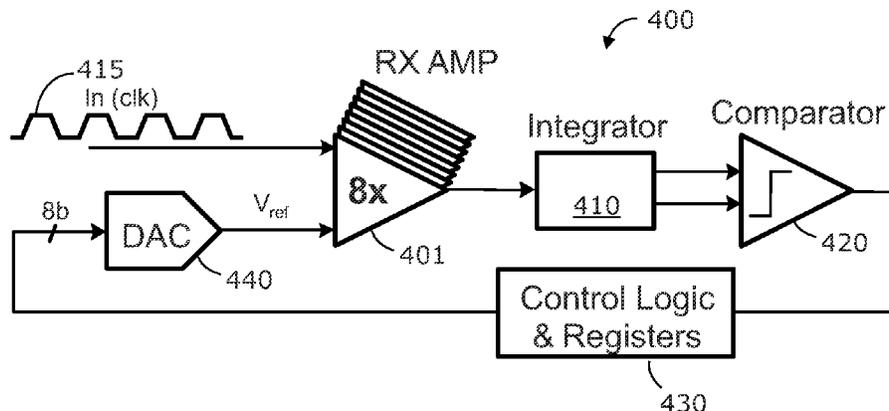
(74) Attorney, Agent, or Firm — Hamilton, Brook, Smith & Reynolds, P.C.

(57)

ABSTRACT

According to at least one example embodiment a two phase calibration approach is employed for calibrating an input/output interface having multiple single-ended receivers. During a first phase, amplifier offset calibration is applied to each of the multiple single-ended receivers. During a second phase, reference voltage calibration is applied to a single-ended receiver of the multiple single-ended receivers to determine a calibration reference voltage value. The calibration reference voltage value is then employed in each of the multiple single-ended receivers during an active phase of the input/output interface.

24 Claims, 9 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

2012/0032722 A1* 2/2012 Mulder H03F 3/45192
327/307
2012/0086494 A1* 4/2012 Asada H03L 7/0807
327/307
2012/0268181 A1 10/2012 Fujimaki
2012/0299653 A1* 11/2012 Scott H04L 25/0272
330/253
2015/0091631 A1 4/2015 Yildirim et al.
2015/0092510 A1 4/2015 Yildirim et al.

OTHER PUBLICATIONS

Hyung-Joon Chi et. Al. "A 3.2Gb/s 8b Single-Ended Integrating DFE RX for 2-Drop DRAM Interface with Internal Reference Voltage and Digital Calibration" Solid-State Circuits Conference, Feb 3-7, 2008,

ISSCC 2008 Digest of Technical Papers, IEEE International, pp. 112-600.

Notice of Allowance mailed Mar. 31, 2015, in U.S. Appl. No. 14/040,563.

Non-Final Office Action dated Aug. 28, 2014 Issued in U.S. Appl. No. 14/040,532.

Non-Final Office Action dated Dec. 15, 2014 Issued in U.S. Appl. No. 14/040,563.

Final Office Action dated Jan. 16, 2015 Issued in U.S. Appl. No. 14/040,532.

Final Office Action dated Nov. 20, 2015, issued in U.S. Appl. No. 14/040,532.

Notice of Allowance for U.S. Appl. No. 14/040,532, entitled: Method and Apparatus For Reference Voltage Calibration In A Single-Ended Receiver, dated May 26, 2016.

* cited by examiner

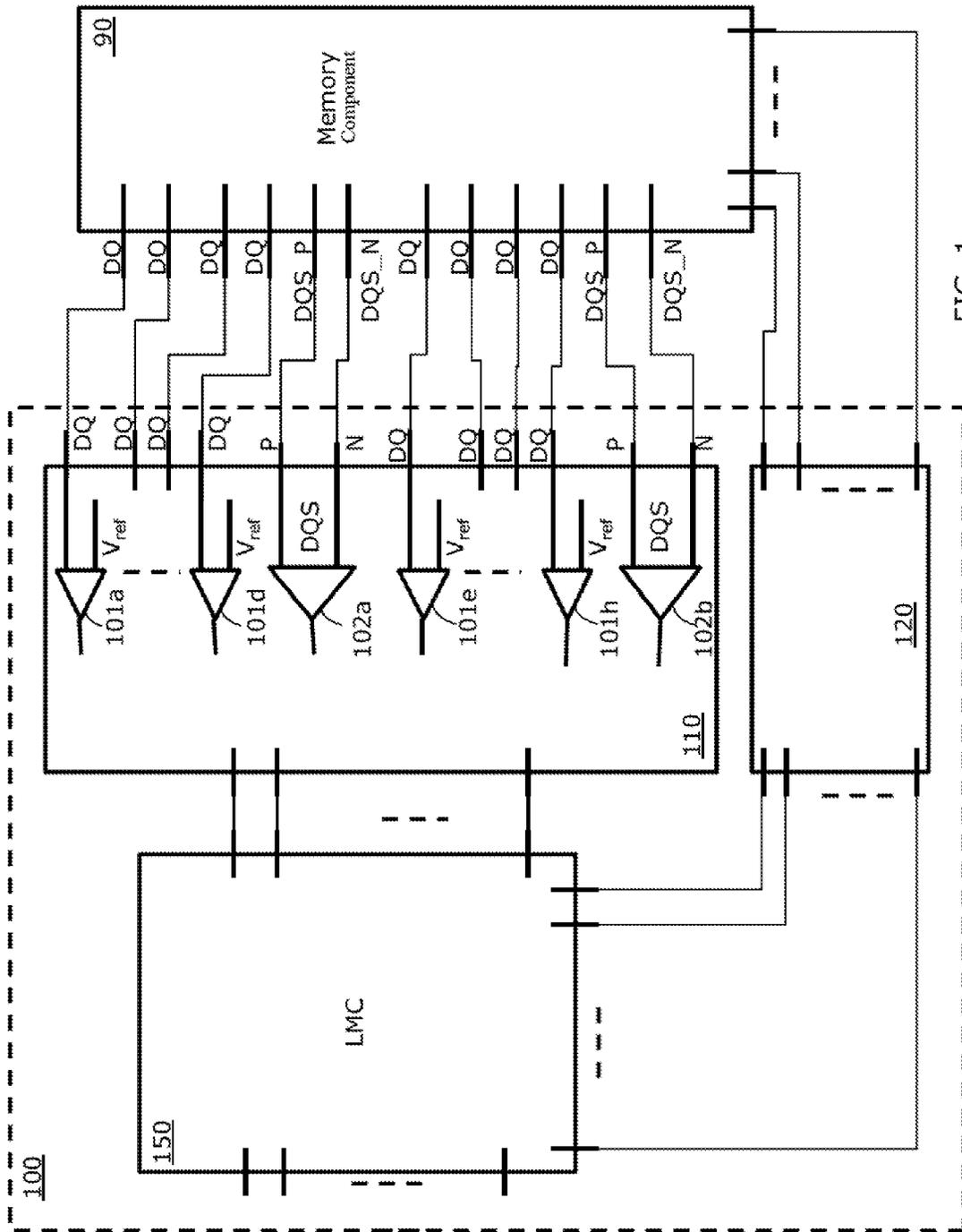


FIG. 1

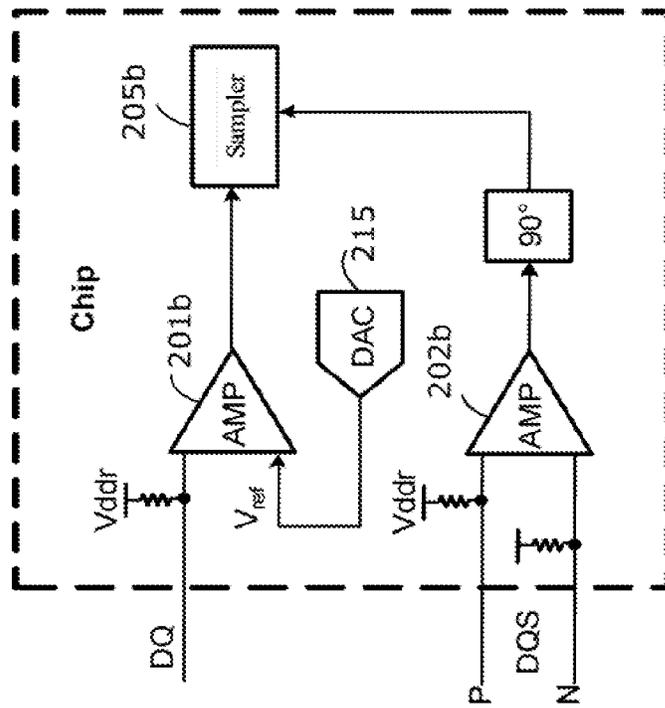


FIG. 2B

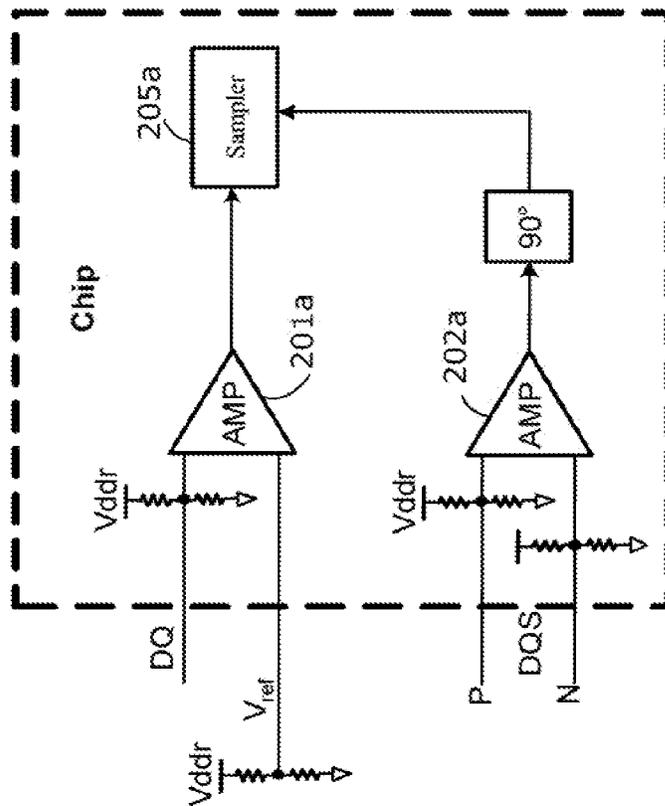


FIG. 2A

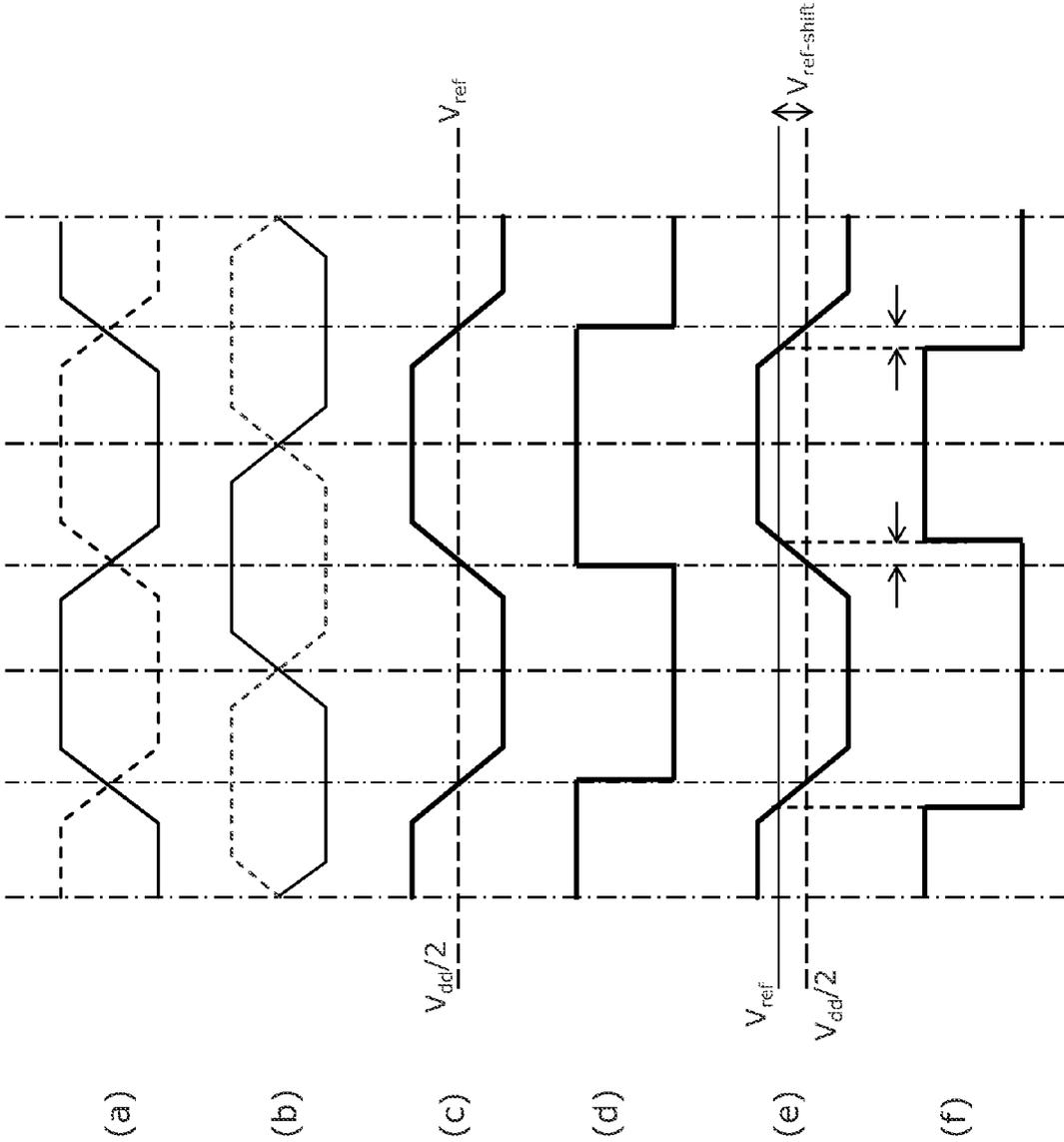


FIG. 3

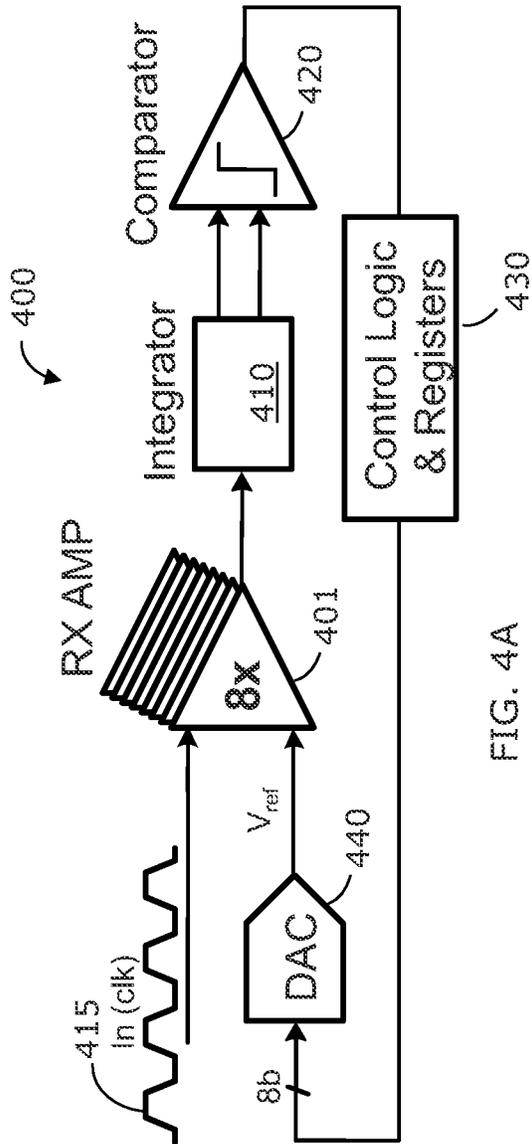


FIG. 4A

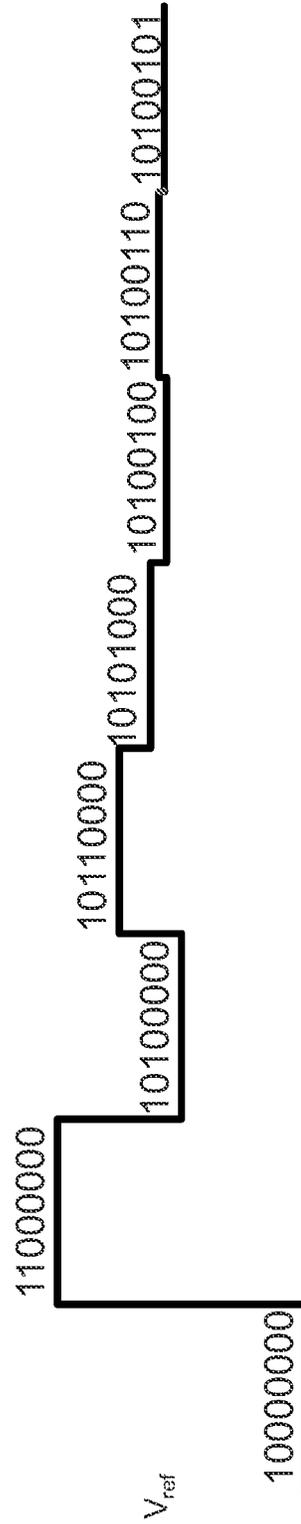


FIG. 4B

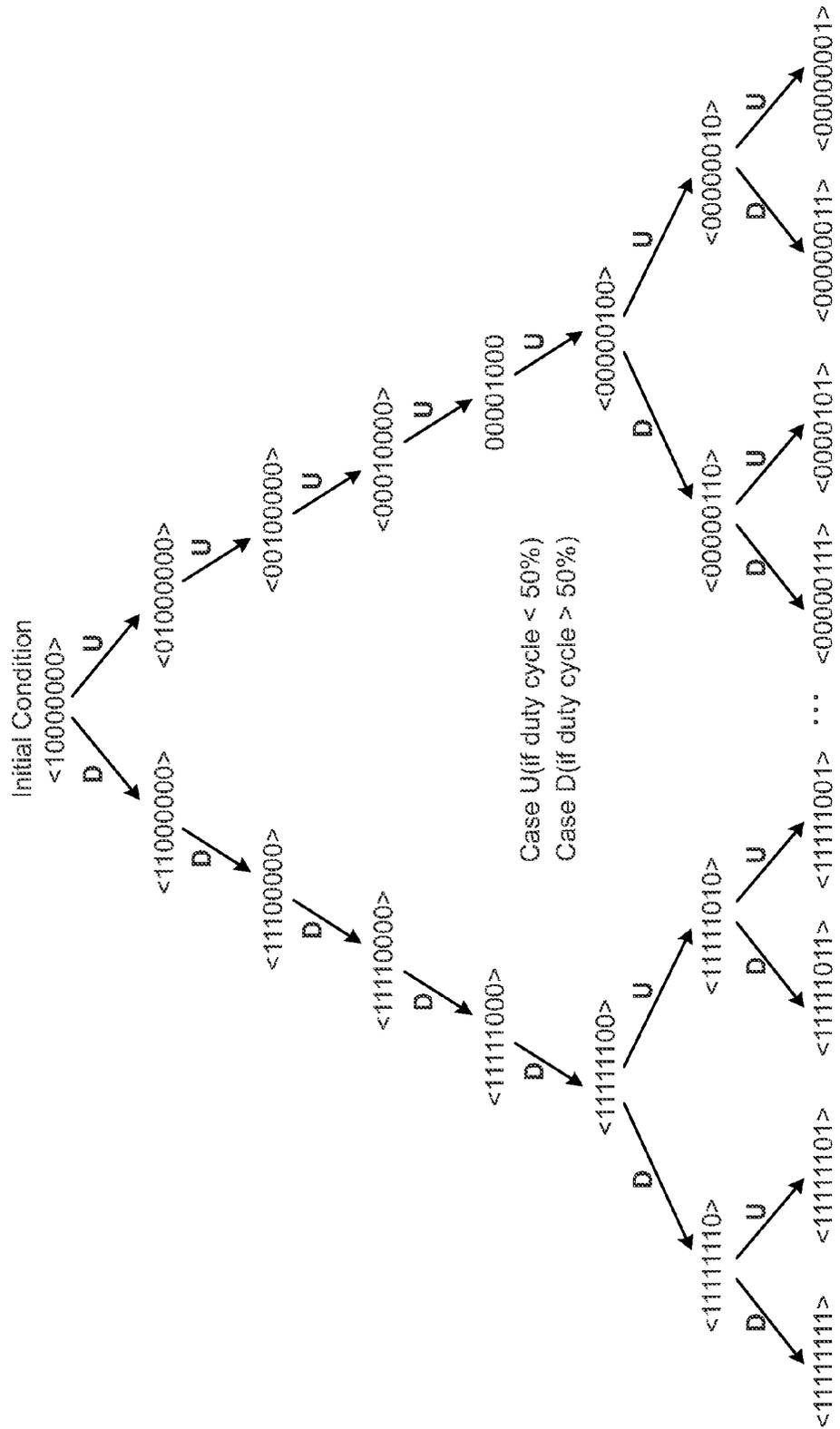


FIG. 5

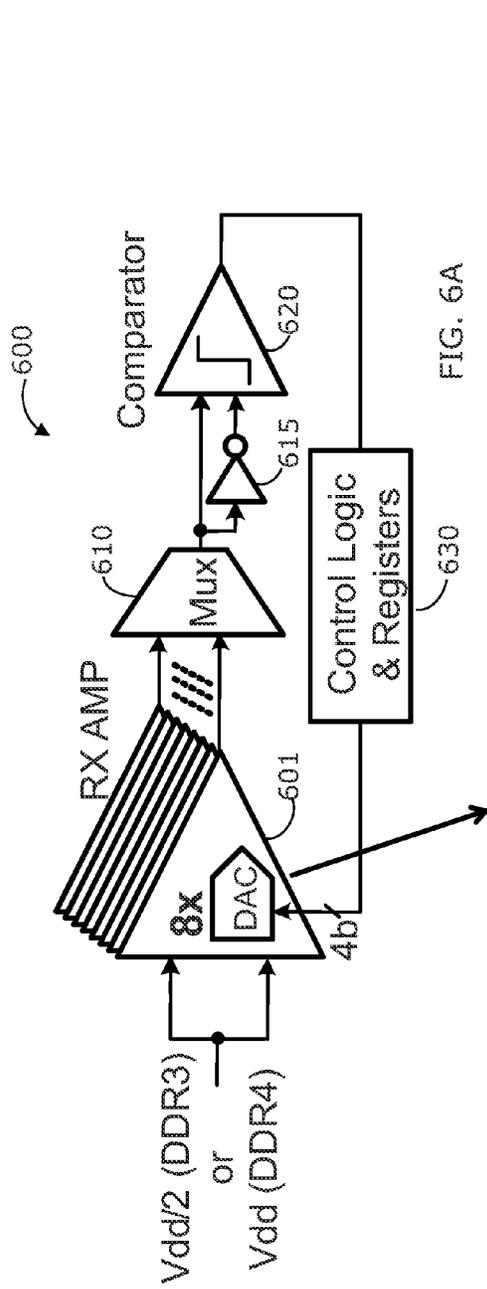


FIG. 6A

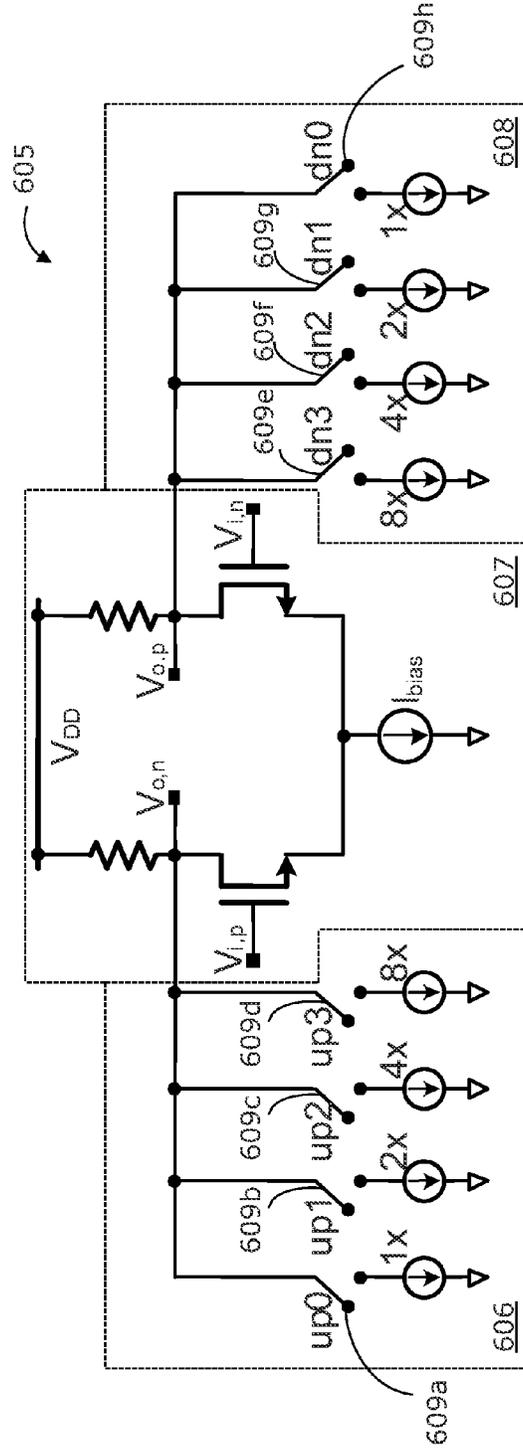


FIG. 6B

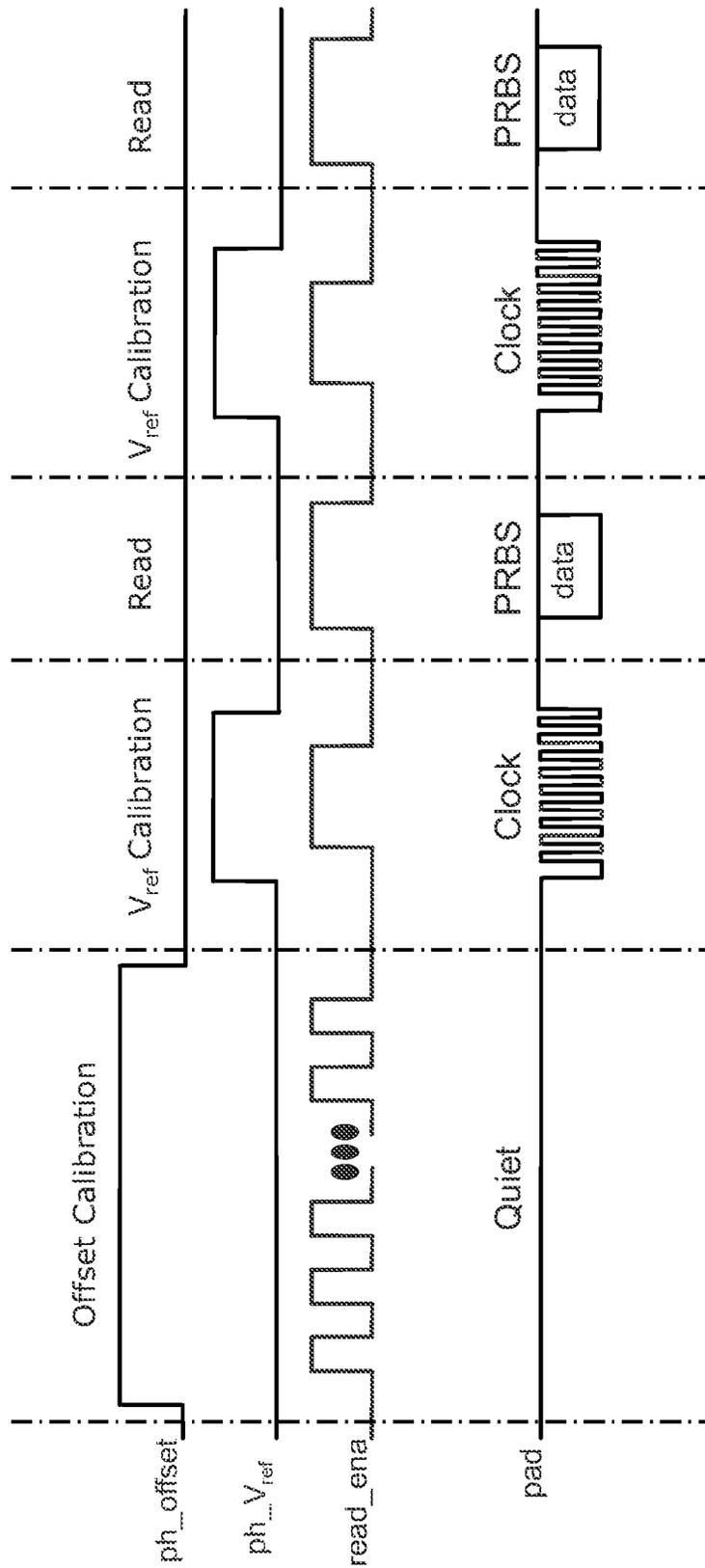


FIG. 8

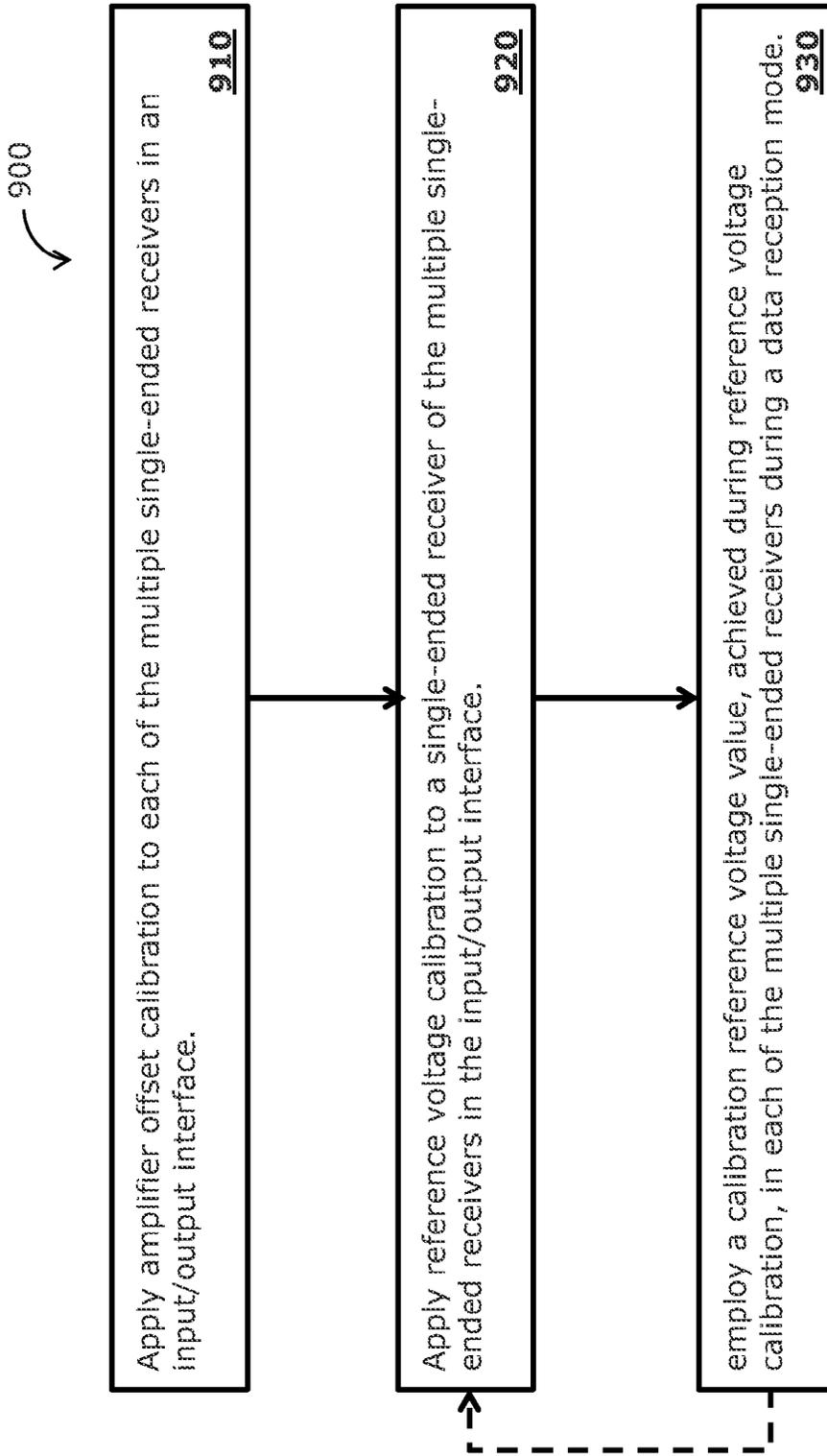


FIG. 9

METHOD AND APPARATUS FOR CALIBRATING AN INPUT INTERFACE

BACKGROUND

Many memory interfaces employ single-ended receivers to receive data from a corresponding memory or other memory interfaces. A single-ended receiver typically includes a differential amplifier having a reference DC voltage and a data signal usually applied as inputs.

SUMMARY

According to at least one example embodiment, a two phase calibration approach is employed for calibrating an input/output interface having multiple single-ended receivers. During a first phase, amplifier offset calibration is applied to each of the multiple single-ended receivers. During a second phase, reference voltage calibration is applied to a single-ended receiver of the multiple single-ended receivers to determine a calibration reference voltage value. The calibration reference voltage value is then employed in each of the multiple single-ended receivers during an active phase, e.g., a data reception phase, of the input/output interface.

In applying amplifier offset calibration, an input value is applied to both input leads of each amplifier associated with a corresponding single-ended receiver of the multiple single-ended receivers, the amplifier including one or more digital-to-analog converters (DACs) used to calibrate an offset of the amplifier. Control logic associated with input/output interface updates, over a number of iterations, a digital value based on an output of the amplifier. The digital value updated is provided as input to a DAC of the one or more DACs in the amplifier. The final value of the digital value, e.g., associated with a last iteration, is employed as input to the DAC of the one or more DACs in the amplifier for calibrating the offset of the amplifier during the active phase of the input/output interface. The one or more DACs are coupled to at least one gain circuit in the corresponding amplifier. In updating the digital value at a first iteration, the DAC for which the corresponding input digital value to be updated is determined. The DAC is determined based on the output of the corresponding amplifier and a coupling of the DAC to a gain circuit in the amplifier.

According to at least one example embodiment, the digital value is updated based on an indication of whether the output of the amplifier is logic 1 or 0. The digital value is represented by multiple bits. The total number of iterations is equal to the number of bits representing the digital value.

According to at least one example embodiment, in applying reference voltage calibration, a clock signal and a reference voltage signal are applied as inputs to an amplifier of the single-ended receiver. An indication of a duty cycle associated with an output signal of the amplifier is evaluated. Control logic associated with input/output interface adjusts a level of the reference voltage signal based on the evaluated indication of the duty cycle. The evaluating and adjusting processes are repeated over a number of iterations.

In adjusting the level of the reference voltage, the control logic, for example, updates over the number of iterations an input digital value to a digital-to-analog converter (DAC), the DAC providing a reference voltage level value to the amplifier. The input digital value is represented by multiple bits. The number of iterations is equal to the number of bits representing the input digital value minus one.

According to at least one example embodiment, the input/output interface is associated with a memory interface, such

as, double data rate 2 (DDR2) memory interface, double data rate 3 (DDR3) memory interface, double data rate 4 (DDR4) memory interface, low power double data rate 2 (LP DDR2) memory interface, low power double data rate 3 (LP DDR3) memory interface, low power double data rate 4 (LP DDR4) memory interface, graphical double data rate 3 (GDDR3) memory interface, graphical double data rate 4 (GDDR4) memory interface, graphical double data rate 5 (GDDR5) memory interface, wide input/output (Wide I/O) memory interface, wide input/output 2 (Wide I/O 2) memory interface, or the like.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. 1 is a diagram illustrating an overview of a memory system, according to at least one example embodiment;

FIGS. 2A and 2B are block diagrams illustrating single-ended receivers associated, respectively, with DDR3 and DDR4 memory interfaces, according to at least one example embodiment;

FIG. 3 is a set of plots illustrating the effect of a reference voltage shift on a corresponding DQ signal;

FIG. 4A is a diagram illustrating a system, or circuit, for reference voltage calibration;

FIG. 4B is a diagram illustrating an example scheme of updating the input of the digital-to-analog converter as part of reference voltage calibration, according to at least one example embodiment;

FIG. 5 is a tree illustrating an algorithm for adapting the input of the digital-to-analog converter as part of reference voltage calibration, according to at least one example embodiment;

FIG. 6A is a diagram illustrating a system, or circuit, for amplifier offset calibration;

FIG. 6B shows a circuit of two digital-to-analog converters coupled to a gain stage of a differential amplifier, according to at least one example implementation;

FIG. 7 is a tree illustrating a scheme according to which a digital input for a DAC, within a differential amplifier of a single-ended receiver, is iteratively updated, according to at least one example embodiment;

FIG. 8 shows a set of plots illustrating different operation phases of a differential amplifier of a single-ended receiver, according to at least one example embodiment; and

FIG. 9 is a flowchart illustrating a method of calibrating an input interface having multiple single-ended receivers, according to at least one example embodiment.

DETAILED DESCRIPTION

A description of example embodiments of the invention follows.

One of the commonly performed operations by a microprocessor is memory access. While microprocessors are getting faster and faster, latency associated with memory access usually results into a performance bottleneck. In fact, memory bottleneck represents a real challenge with respect to improving the performance of a processing system. One way to reduce latency associated with memory access operations

is to enhance performance and accuracy of the memory interface associated with the accessed memory.

Many memory interfaces make use of single-ended receivers. Examples of such memory interfaces include double data rate 2 (DDR2) interface, DDR3 interface, DDR4 interface, low power double data rate 2 (LPDDR2) interface, LPDDR3 interface, LPDDR4 interface, graphical double data rate 3 (GDDR3) interface, GDDR4 interface, GDDR5 interface, wide input/output (Wide I/O) interface, and Wide I/O 2 interface.

FIG. 1 is a diagram illustrating an overview of a memory system according to at least one example embodiment. The memory system includes a memory controller device **100** and a memory component **90**. The memory controller device is typically implemented within a microprocessor. In response to a read operation, the memory component **90** outputs eight data signals, also referred to as DQ signals, representing eight bits of a data byte, and at least one pair of data strobe signals, also referred to as DQS signals. In the example shown in FIG. 1, each four DQ signals are associated with a corresponding DQS signal. The memory controller device **100** includes a bidirectional input/output memory interface **110**, a unidirectional command interface **120**, and a local memory controller LMC **150**. The command interface is an output-only interface for sending commands from the LMC **150** to the memory component **90**. The input/output memory interface **110** is a bidirectional I/O interface for sending data, in both directions, between the memory component **90** and the LMC **150**. The I/O memory interface **110** includes eight single-ended receivers, each having a differential amplifier, e.g., **101a-101h**. For the sake of simplicity, the single-ended receivers **101a-101h** are shown with respect to one direction of data transfer between the memory component **90** and the LMC **150**. For each of the differential amplifiers **101a-101h**, associated with the single-ended receivers, the corresponding inputs include a reference voltage (V_{ref}) and one of the DQ signals, e.g., provided by the memory component **90**. The I/O memory interface **110** also includes at least one other differential amplifier, e.g., **102a** and **102b**. Each of the differential amplifiers **102a** and **102b** is coupled to one pair of DQS signals as inputs. Output of the I/O memory interface **110** is provided to a microprocessor, e.g., to a level-2 cache (L2C) of the microprocessor, through the local memory controller **150**. The output-only command interface **120**, receives input signals from the local memory controller **150** and provides corresponding output signals to the memory component **90**.

FIGS. 2A and 2B are block diagrams illustrating single-ended receivers associated, respectively, with DDR3 and DDR4 memory interfaces, according to at least one example embodiment. In the DDR3 memory interface shown in FIG. 2A, each input node of a differential amplifier **201a** of the single-ended receiver is coupled to two resistors. Also, each input node of a differential amplifier **202a**, receiving a pair of DQS signals, is coupled to two resistors. The output of the differential amplifier **202a** is shifted by 90 degrees. The shifted output of the differential amplifier **202a** and the output of the differential amplifier **201a** are provided to a sampler **205a**. The sampler **205a** is configured to sample the output of the differential amplifier **201a** based on the shifted output of the differential amplifier **202a**. The output of the sampler **205a** is provided to the local memory controller **150**.

In the DDR4 memory interface shown in FIG. 2B, the DQ input node of a differential amplifier **201b** of the single-ended receiver is coupled to a single resistor. Also, the DQS_P input node of a differential amplifier **202b**, receiving a DQS_P signal, is coupled to a single resistor. The reference voltage input to the differential amplifier **201b** is defined by a digital-

to-analog converter (DAC) **215**. Similar to the DDR3 memory interface, the output of the differential amplifier **202b** is shifted by 90 degrees. The shifted output of the differential amplifier **202b** and the output of the differential amplifier **201b** are provided to a sampler **205b**. The sampler **205b** is configured to sample the output of the differential amplifier **201b** based on the shifted output of the differential amplifier **202b**. The output of the sampler **205b** is provided to the local memory controller **150**.

Degradation in the performance of a memory interface, e.g., DDR I/O memory interface such as **110**, may be due to a shift in the reference voltage V_{ref} or amplifier offset. Amplifier offset within a differential amplifier, e.g., **101a**, **101b**, . . . , or **101h**, results in an internal potential difference between the two input nodes of the differential amplifier even when the same voltage is applied to both nodes. The shift in the reference voltage and/or the amplifier offset within one or more differential amplifiers may be caused, for example, by Process-Voltage-Temperature (PVT) variation, design of the board on which the integrated circuit(s) (IC) resides, or other factors.

FIG. 3 is a set of plots illustrating the effect of a reference voltage shift on a corresponding DQ signal. Plot (a) shows DQS signals while plot (b) shows the same DQS signals shifted by 90 degrees. The plot (c) shows a DQ signal associated with the DQS signals in the plots (a) and (b). The DQ signal in plot (c) and the DQS signals shown in plot (a) are edge-aligned with each other. By shifting the DQS signals as shown in plot (b), the fall and rise phases of the shifted DQS signals become aligned with the middle of the pulse duration of the DQ signal in plot (c). The DQ signal in plot (c) has a reference voltage V_{ref} equal to half of the corresponding supply voltage, i.e., $V_{dd}/2$, therefore resulting in equal pulse durations for distinct DQ pulses as shown in plot (d). Plot (e), however, shows a shift in the reference voltage equal to $V_{ref-shift}$ with respect to half the supply voltage, e.g., $V_{ref-shift} = V_{ref} - (V_{dd}/2)$. The shift in the reference voltage may result in non-equal pulse durations for distinct DQ pulses. A person skilled in the art should appreciate that an offset in internal amplifier voltage may lead to similar effects as the ones caused by a shift in the reference voltage but with relatively smaller range. That is, an offset in internal amplifier voltage may potentially cause non-uniform pulse duration across distinct DQ pulses, increased duty cycle distortion, and/or potentially higher sampling error rate by the sampler **150**. However, the effects of an offset in internal amplifier voltage are typically less severe in magnitude than the effects of a shift in the reference voltage.

In typical memory interfaces, amplifier reference voltage is addressed through amplifier reference voltage calibration that is usually handled by the software of the microprocessor which causes the local memory controller **150** to take specific actions. Specifically, the software causes the LMC **150** to instruct the memory component **90** to send one or more patterns of DQ bits, e.g., eight bits, to the I/O memory interface **110** over a number of iterations. The corresponding outputs from the I/O memory interface **110** are compared to expected data patterns and an estimate of the reference voltage is evaluated based on comparison results over the iterations. For an eight-bit reference voltage calibration, the number of iterations is equal to 256 iterations to cover the entire code range.

According to at least one example embodiment, a scheme of reference voltage calibration is performed within the I/O memory interface **110**. According to at least one other example embodiment, a scheme of amplifier offset calibration is performed within the I/O memory interface **110**. The reference voltage calibration process and the amplifier offset

calibration process are not handled by the local memory controller 150. Specifically, the reference voltage calibration and/or the amplifier offset calibration may be triggered by the LMC 150, however, the calibration processes, e.g., adjustment of calibration parameters, are performed within the I/O memory interface 110 with no control interference from the LMC 150. According to further example embodiment(s) a two-phase amplifier calibration is performed. During a first phase, amplifier offset calibration is applied to each single ended receiver of the I/O memory interface 110. In a second stage, a reference voltage calibration is applied to at least one single-ended receiver of the I/O memory interface 110.

FIG. 4A is a diagram illustrating a system, or circuit, 400 for reference voltage calibration. The system 400 includes a differential amplifier 401 of a single-input receiver, integrator circuit 410, comparator 420, control logic 430, and digital to analog converter (DAC) 440. The DAC 440 converts a digital value into an analog voltage value that is applied to the differential amplifier 401 as a reference voltage. The digital value, e.g., an eight-bit digital value, is provided by the control logic 430. A clock signal 405 is applied to the differential amplifier 401 as a second input besides the reference voltage. The output of the differential amplifier is fed to the integrator 430. The integrator circuit 410 is configured to provide one or more values indicative of the duty cycle associated with the output signal of the differential amplifier 401.

According to an example implementation, the integrator circuit 410 may generate two signals from the output signal of the differential amplifier 401; a first generated signal consisting of high-voltage pulses of the amplifier's output signal, and a second generated signal consisting of low-voltage pulses of the amplifier's output signal. The integrator circuit 410 then integrates each of the generated signals over a time interval and provides two corresponding integral values to the comparator 420. The comparator compares the two values and provides an indication of the result of comparison to the control logic 430. Alternatively, the integrator may compute an estimate of the duty cycle based on the computed integral values and provide the duty cycle estimate result to the comparator 420. The comparator then compares the estimated duty cycle to a reference duty cycle value, e.g., 50%, and provides the result of the comparison to the control logic 430. The control logic 430 is a hardware logic, or logic circuit.

According to another example implementation, the integrator circuit 410 may simply integrate the amplifier's output signal over a period of time equal to a number of clock cycles, and provide an indication of the integration result to the comparator 420. The comparator 420 compares the indication of the integration result to zero or to its inverted value, and provides an indication of the comparison result to the control logic 430.

Based on the received indication of the comparison result, the control logic 430 is configured to determine whether the reference voltage is to be increased or decreased. For example, an indication that the duty cycle is less than 50%, e.g., the duration of a high voltage pulse is smaller than the duration of a low voltage pulse in the output signal from the differential amplifier, suggests that there is a positive shift in the reference voltage and that the reference voltage needs to be decreased. However, an indication that the duty cycle is greater than 50% suggests that there is a negative shift in the reference voltage and that the reference voltage is to be increased. Based on the determined type of shift in the reference voltage, e.g., positive or negative, the control logic 430 updates the digital value representing the reference voltage and provides the updated digital value to the DAC 440. The DAC 440 converts the digital value to an analog DC voltage.

The DC voltage is fed to the differential amplifier 401 as an updated reference voltage. Such process is repeated for a number of iterations before reaching a final value of the reference voltage.

FIG. 4B is a diagram illustrating an example scheme of updating the input of the digital-to-analog converter 440 as part of reference voltage calibration, according to at least one example embodiment. The control logic 430 applies a binary, or half-interval, search. Assuming that the digital value is an eight-bit number, the control logic 430 starts with the binary number 10000000, or 128, to initialize the digital value. When applying the reference voltage corresponding to the initial digital value, the control logic 430 detects that the duty cycle is greater than 50%, and increases the digital value to 11000000. With the new digital value, the duty cycle is determined to be less than 50% and the digital value is decreased to 10100000. The process continues until a final value of the digital value, e.g., 10100101, is achieved after seven iterations. In general, if the number of bits representing the digital value is n , the binary search algorithm takes only $n-1$ iterations to achieve a final result.

FIG. 5 is a tree graph illustrating an algorithm for adapting the input of the digital-to-analog converter in reference voltage calibration, according to at least one example embodiment. In the tree graph shown in FIG. 5, only eight paths out of a total of 128 potential paths of the binary search algorithm for an eight-bit binary number are shown. Each node of the tree represents a digital value indicative of a corresponding analog reference voltage value. Each edge in the tree is either marked with "U," indicating that a current reference voltage value suggests a shift up, or positive shift, and that the reference voltage value is to be decreased in the next iteration, or marked with "D," indicating a down shift, or negative shift, of the current reference voltage and that the current reference voltage value is to be decreased.

A person skilled in the art should appreciate that a reference duty cycle value other than 50% may also be used, e.g., if the clock signal 415 fed to the differential amplifier has a duty cycle different from 50%. In other words, the reference duty cycle value considered when performing the comparison at the comparator 420 is equal to the duty cycle of the clock signal 415. Also, it should be appreciated that reference voltage calibration is applied to at least one single-ended receiver among the multiple single ended receivers, for example, within the I/O memory interface 110. For example, reference voltage calibration may be applied to one single-ended receiver. At the end of the reference voltage calibration process, the final reference voltage is applied to all differential amplifiers, e.g., 101a-101h, associated with multiple single-ended receivers within the I/O memory interface 110.

FIG. 6A is a diagram illustrating a system, or circuit, 600 for amplifier offset calibration. The system 600 includes multiple differential amplifiers 601 associated with multiple single-input receivers. According to at least one example embodiment, amplifier offset calibration is applied to each amplifier of the multiple single-ended receivers within the I/O memory interface 110. For each differential amplifier associated with a corresponding single-ended receiver, the same DC voltage is applied to both input nodes of the differential amplifier during the process of amplifier offset calibration. The system 600 also includes at least one multiplexer 610 and a comparator 620. According to at least one example implementation, outputs from multiple differential amplifiers 601 are multiplexed serially by the multiplexer 610. Each output is then inverted by an inverter 615, and both the output and its inverted value are passed to the comparator 420. The comparator 420 compares both values and provides an indication

of the comparison result to control logic 630. The control logic 630 is hardware logic, or logic circuit, and is configured to update a digital value for sending to a DAC within a differential amplifier 601 based on the comparison result. The DAC is within the differential amplifier 601 whose output is used to generate the indication of the comparison result. In other words, given an indication of the result of comparison corresponding to a given differential amplifier 601, the control logic 630 determines whether a digital input value, associated with a DAC within the same differential amplifier 601, is to be increased or decreased based on the indication of the comparison result received from the comparator 620. The control logic 630 then sends an updated value of the input digital value to the DAC with the differential amplifier 601. The process of using the output of the differential amplifier 601 to update the input digital value associated with a DAC within the same differential amplifier 601 is repeated for a number of iterations.

FIG. 6B shows a circuit 605 of two digital-to-analog converters coupled to a gain stage of a differential amplifier 601, according to at least one example implementation. According to the example implementation shown in FIG. 6B, each DAC is a four-bit DAC. A first DAC 606 is coupled to one side of the second stage gain 607 of the differential amplifier 601, and a second DAC 608 is coupled to a second side of the second stage gain 607 of the differential amplifier 601. By updating the digital input value of a DAC, e.g., 606 or 608, the control logic 630 is configuring the switches, e.g., 609a-609d or 609e-609h, associated with the same DAC.

A person skilled in the art should appreciate that one or more DACs, within a given differential amplifier 601, may be configured by the control logic 630. For example, assuming that the differential amplifier has a number of gain stages, the one or more DACs may be arranged in a way to be coupled to any of the gain stages of the differential amplifier 601. For example, a total of two DACs may be configured by the control logic 630. The two DACs may be both coupled the second gain stage of the differential amplifier, as shown in FIG. 6B, or any other gain stage of the differential amplifier. Alternatively, each DAC may be couple to a distinct gain stage. According to another example implementation, more than two DACs may be configured by the control logic 630. In such case different coupling patterns between the two or more DACs and gain stages of the differential amplifier 601 may also be considered. According to yet another example implementation, only a single DAC, coupled to a gain stage of the differential amplifier 601, may be configured by the control logic.

FIG. 7 is a tree 700 illustrating a scheme according to which a digital input for a DAC, within a differential amplifier 601 of a single-ended receiver, is iteratively updated, according to at least one example embodiment. The tree 700 corresponds to a scenario where two DACs, e.g., as shown in FIG. 6B, are configurable by the control logic 630. Initially, e.g., at the first iteration, the digital value associated with each of the DACs is initialized to 0000. Upon receiving an indication of the comparison result associated with the output of the differential amplifier 601, the control logic determines which DAC is to be configured based on the received indication.

For example, if it is determined that the differential amplifier 601 has a negative voltage offset initially, e.g., the output of the differential amplifier 601 is negative, and the output voltage is to be increased, the DAC 606 in FIG. 6B is the one selected for configuration. Specifically the digital input value applied to DAC 606 is updated to be 1000 while the digital input value applied to the DAC 608 is kept 0000. The selection of the DAC 606 is illustrated in the tree 700 by the node

715a. However, if it is determined that the differential amplifier 601 has a positive voltage offset initially, e.g., the output of the differential amplifier 601 is positive, and the output voltage is to be decreased, the DAC 608 in FIG. 6B is the one selected for configuration. The digital input value applied to DAC 608 is updated to be 1000 while the digital input value applied to the DAC 606 is kept 0000. The selection of the DAC 608 is illustrated in the tree 700 by the node 715b.

Once a DAC is selected, the digital input value for the selected DAC is updated in the following iterations. For example, the digital input value for the selected DAC is updated according to a binary, or half-interval, search algorithm as illustrated in the tree 700. In other words, at each iteration, the digital input value is updated by a half of an interval representing a range of update values. In the tree 700, an edge marked as “U” indicates an update towards increasing the offset voltage, and an edge marked as “D” indicates an update towards decreasing the offset voltage of the differential amplifier 601. A person skilled in the art should appreciate that the updating of the digital input value may be performed according to a different scheme other than the binary search approach.

FIG. 8 shows a set of plots illustrating different operation phases of a differential amplifier 601 of a single-ended receiver, according to at least one example embodiment. According to at least one example embodiment, the offset calibration is performed when power is turned on, as shown by the offset phase plot “ph_offset,” so that offset of each receiver amplifier due to the non-uniformity and PVT variation is compensated. Offset calibration is performed to each differential amplifier of a single-ended receiver within the I/O memory interface 110. Once amplifier offset calibration is completed, reference voltage calibration is performed, as shown in the reference voltage calibration phase plot “ph_V_{ref}” for at least one single-ended receiver, e.g., within the I/O memory interface 110. Upon completion of the reference voltage calibration, the final reference voltage is applied, e.g., to all differential amplifiers associated with single-ended receivers within the I/O memory interface 110. After reference voltage calibration is complete, data read operations are performed. According to at least one example implementation, the reference voltage calibration process may be repeated during idle phases of the single-ended receivers. Also, during offset calibration, the enable read signal “ena_read” may be employed as the clock signal fed to control logic 630 and comparator 620.

A person skilled in the art should appreciate that embodiment of the amplifier offset calibration and the reference voltage calibration described above may also be applied in I/O interfaces that are not memory interfaces.

FIG. 9 is a flowchart illustrating a method 900 of calibrating an I/O interface having multiple single-ended receivers, according to at least one example embodiment. At block 910, amplifier offset calibration is applied to each of the multiple single-ended receivers in the I/O interface. The amplifier offset calibration is achieved through an iterative approach as described with respect to FIGS. 6A, 6B, and 7. Specifically, the same DC voltage is applied to both inputs of the differential amplifier of each single-ended receiver. Based on the sign of the output, a control logic 630 configures switches associated with a DAC within the differential amplifier. Configuring the switches of the DAC is achieved by updating a digital value provided as input to the DAC. According to an example embodiment, more than one DACs within each differential amplifier may be configurable by the control logic 630. For example, in a first iteration, the control logic determines one

of the DACs to be configured. In the following iterations, a digital value provided as input to the DAC determined is updated.

Once amplifier offset calibration is complete, reference voltage calibration is applied, at block 920, to at least one single-ended receiver of the multiple single-ended receivers to determine a calibration reference voltage value. Reference voltage calibration is performed iteratively as illustrated above in the description of FIGS. 4A, 4B, and 5. In other words, a DC voltage signal and a clock signal are applied as inputs to the differential amplifier of the single-ended receiver. The output of the differential amplifier is analyzed to determine an indication of the corresponding duty cycle, e.g., greater or less, than a reference value. Based on the determined indication of the duty cycle, a control logic 430 updates a digital value provided as input a DAC 440. The digital value represents an updated value of the reference voltage level, and is converted to an analog DC voltage by the DAC 440. The DC voltage is applied as the reference voltage to the differential amplifier. The analyzing and updating process is repeated over a number of iterations, e.g., equal to the number of bits representing the digital number minus one, and a final reference voltage level is achieved at the last iteration.

At block 930, the final reference voltage level is applied within each of the multiple single-ended receivers during a data reception mode. According to an example implementation, the reference voltage calibration may be repeated at a later time during an idle mode of the input/output interface. The amplifier offset calibration is performed after starting the chip associated with the input/output interface.

A person skilled in the art should appreciate that the amplifier offset calibration and the reference voltage calibration embodiments described above may also be applied in systems/circuits other than input/output interfaces and memory interfaces.

While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. A method of calibrating an input/output interface having multiple single-ended receivers, the method comprising:
 - applying amplifier offset calibration to each of the multiple single-ended receivers during a first phase, each single ended receiver including an amplifier, the amplifier offset calibration iteratively determines a value for calibrating an internal voltage offset of the amplifier of each of the multiple single-ended receivers to produce a determined value;
 - employing the determined value for each amplifier to the amplifier corresponding to each of the multiple single-ended receivers during an active phase of the input/output interface;
 - applying reference voltage calibration to one single-ended receiver of the multiple single-ended receivers to determine a calibration reference voltage value during a second phase; and
 - employing the calibration reference voltage value determined for the one single-ended receiver in each of the multiple single-ended receivers during the active phase of the input/output interface.
2. The method as recited in claim 1, wherein applying amplifier offset calibration includes:

applying an input value to both input leads of the amplifier associated with a corresponding single-ended receiver of the multiple single-ended receivers, the amplifier including one or more digital-to-analog converters (DACs) used to calibrate the internal voltage offset of the amplifier; and

updating, over a number of iterations by a control logic coupled to the amplifier, a digital value based on an output of the amplifier, the digital value updated being provided as input to a DAC of the one or more DACs in the amplifier,

a final value of the digital value is employed as input to the DAC of the one or more DACs in the amplifier for calibrating the internal voltage offset of the amplifier during a data reception phase.

3. The method as recited in claim 2, wherein the one or more DACs are coupled to at least one gain circuit in the amplifier.

4. The method as recited in claim 2, wherein updating the digital value at a first iteration includes determining the DAC, from the one or more DACs, associated with the digital value.

5. The method as recited in claim 4, wherein determining the DAC associated with the digital value includes determining the DAC based on the output of the amplifier and a coupling of the DAC to a gain circuit in the amplifier.

6. The method as recited in claim 2, wherein updating the digital value based on the output of the amplifier includes updating the digital value based on an indication of whether the output of the amplifier is logic 1 or 0.

7. The method as recited in claim 2, wherein the digital value is represented by multiple bits.

8. The method as recited in claim 2, wherein the number of iterations is equal to a number of bits representing the digital value.

9. The method as recited in claim 1, wherein applying reference voltage calibration includes:

applying a clock signal and a reference voltage signal as inputs to the amplifier associated with the one single-ended receiver of the multiple single-ended receivers;

evaluating an indication of a duty cycle associated with an output signal of the amplifier;

adjusting, by control logic, a level of the reference voltage signal based on the evaluated indication of the duty cycle; and

repeating said evaluating and said adjusting over a number of iterations.

10. The method as recited in claim 9, wherein adjusting the level of reference voltage signal includes setting, by the control logic, an input digital value to a digital-to-analog converter (DAC), the DAC providing a reference voltage level value to the amplifier.

11. The method as recited in claim 10, wherein the input digital value is represented by multiple bits.

12. The method as recited in claim 10, wherein the number of iterations is equal to the number of bits representing the input digital value minus one.

13. The method as recited in claim 1, wherein applying reference voltage calibration is repeated during an idle state of the input/output interface.

14. The method as recited in claim 10, wherein the input/output interface is associated with a memory interface, the memory interface is:

- a double data rate 2 (DDR2) memory interface; a double data rate 3 (DDR 3) memory interface;
- a double data rate 4 (DDR4) memory interface; a low power double data rate 2(LP DDR2) memory interface;

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a low power double data rate 3 (LP DDR3) memory interface;
 a low power double data rate 4 (LP DDR4) memory interface;
 a graphical double data rate 3 (GDDR3) memory interface;
 a graphical double data rate 4 (GDDR4) memory interface;
 a graphical double data rate 5 (GDDR5) memory interface;
 a wide input/output (Wide I/O) memory interface; or
 a wide input/output 2 (Wide I/O 2) memory interface.

15. An input/output interface having multiple single-ended receivers, the input/output interface comprising:

an amplifier in each single ended receiver of the multiple single-ended receivers; and
 a control logic,

the amplifiers and the control logic being configured to:
 apply amplifier offset calibration to each of the amplifiers during a first phase, the amplifier offset calibration iteratively determines a value for calibrating an internal voltage offset of the amplifier of each of the multiple single-ended receivers to produce a value;
 employing the determined value for each amplifier to the amplifier corresponding to each of the multiple single-ended receivers during an active phase of the input/output interface;
 apply reference voltage calibration to one single-ended receiver of the multiple single-ended receivers to determine a calibration reference voltage value during a second phase; and
 employ the calibration reference voltage value determined for the one single-ended receiver in each of the multiple single-ended receivers during the active phase of the input/output interface.

16. The input/output interface as recited in claim 15, wherein each amplifier of the multiple single-ended receivers includes one or more digital-to-analog converters (DACs) with corresponding input of each amplifier of the multiple single-ended receivers used to calibrate an amplifier offset, the control logic being configured to update, over a number of iterations, a digital value for each amplifier of the multiple single-ended receivers based on an amplifier output, the digital value updated being provided as input to a DAC of the one or more DACs,

a final value of the digital value updated being employed as input to the DAC of the one or more DACs for calibrating the amplifier offset during the active phase of the input/output interface.

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17. The input/output interface as recited in claim 16, wherein the one or more DACs in each amplifier are coupled to at least one gain circuit.

18. The input/output interface as recited in claim 16, wherein updating the digital value at a first iteration includes determining DAC, from the one or more DACs, associated with the digital value.

19. The input/output interface as recited in claim 16, wherein the number of iterations is equal to a number of bits representing the digital value.

20. The input/output interface as recited in claim 15, wherein in applying reference voltage calibration, an amplifier of each single-end receiver is configured to provide an output signal in response to a clock signal and a reference voltage signal being applied as inputs to the amplifier, and the control logic configured to adjust, for a number of iterations, a level of the reference voltage signal based on an evaluated indication of a duty cycle associated with the output signal.

21. The input/output interface as recited in claim 20, wherein in adjusting the level of reference voltage signal, the control logic is configured to update an input digital value to a digital-to-analog converter (DAC), the DAC providing a reference voltage level value to the amplifier.

22. The input/output interface as recited in claim 20, wherein the number of iterations is equal to the number of bits representing the input digital value minus one.

23. The input/output interface as recited in claim 15, wherein the input/output interface is configured to repeat applying reference voltage calibration during an idle state of the input/output interface.

24. The input/output interface as recited in claim 15, wherein the input/output interface is associated with a memory interface, the memory interface includes:
 a double data rate 2 (DDR2) memory interface;
 a double data rate 3 (DDR3) memory interface;
 a double data rate 4 (DDR4) memory interface;
 a low power double data rate 2 (LP DDR2) memory interface;
 a low power double data rate 3 (LP DDR3) memory interface;
 a low power double data rate 4 (LP DDR4) memory interface;
 a graphical double data rate 3 (GDDR3) memory interface;
 a graphical double data rate 4 (GDDR4) memory interface;
 a graphical double data rate 5 (GDDR5) memory interface;
 a wide input/output (Wide I/O) memory interface; or
 a wide input/output 2 (Wide I/O 2) memory interface.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,413,568 B2
APPLICATION NO. : 14/040577
DATED : August 9, 2016
INVENTOR(S) : Omer O. Yildirim et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In Column 10, Claim 14, line 65, delete "(DDR 3)" and insert --(DDR3)--;

In Column 10, Claim 14, line 68, delete "interface:" and insert --interface;--;

In Column 12, Claim 18, line 6, delete "determining DAC" and insert --determining the DAC--;

In Column 12, Claim 20, line 13, delete "single-end" and insert --single-ended--;

In Column 12, Claim 23, line 27, delete "Wherein" and insert --wherein--.

Signed and Sealed this
Twenty-fifth Day of October, 2016



Michelle K. Lee
Director of the United States Patent and Trademark Office