US009130162B2

(12) **United States Patent**
**Tu et al.**

(10) **Patent No.: US 9,130,162 B2**
(45) **Date of Patent: Sep. 8, 2015**

(54) **RESISTANCE VARIABLE MEMORY STRUCTURE AND METHOD OF FORMING THE SAME**

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( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/722,466**

(22) Filed: **Dec. 20, 2012**

(65) **Prior Publication Data**

US 2014/0175366 A1 Jun. 26, 2014

(51) **Int. Cl.**
***H01L 45/00*** (2006.01)
***H01L 27/24*** (2006.01)

(52) **U.S. Cl.**
CPC ..... ***H01L 45/1253*** (2013.01); ***H01L 27/2436*** (2013.01); ***H01L 27/2463*** (2013.01); ***H01L 45/08*** (2013.01); ***H01L 45/124*** (2013.01); ***H01L 45/14*** (2013.01); ***H01L 45/146*** (2013.01); ***H01L 45/1608*** (2013.01); ***H01L 45/1675*** (2013.01)

(58) **Field of Classification Search**
CPC ..... H01L 45/146; H01L 45/1608; H01L 45/1253
USPC ..... 257/296–309, 905–908, 25
See application file for complete search history.

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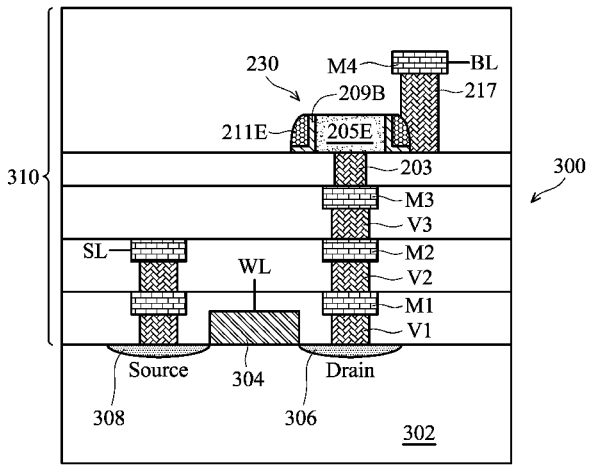
(57) **ABSTRACT**

A semiconductor structure includes a resistance variable memory structure. The semiconductor structure also includes a dielectric layer. The resistance variable memory structure is over the dielectric layer. The resistance variable memory structure includes a first electrode disposed over the dielectric layer. The first electrode has a sidewall surface. A resistance variable layer has a first portion which is disposed over the sidewall surface of the first electrode and a second portion which extends from the first portion away from the first electrode. A second electrode is over the resistance variable layer.

**19 Claims, 7 Drawing Sheets**



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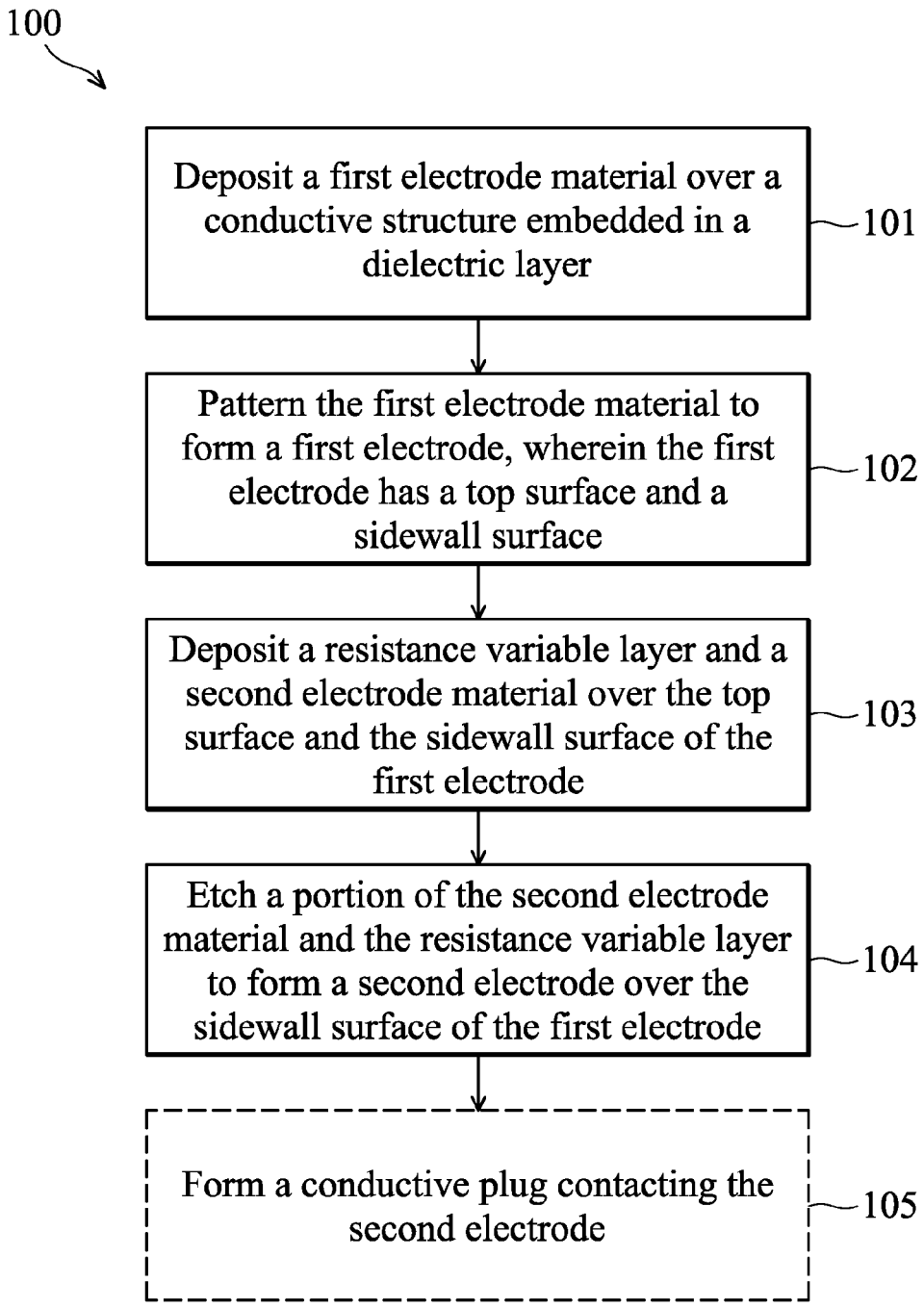
100
Deposit a first electrode material over a conductive structure embedded in a dielectric layer
101
Pattern the first electrode material to form a first electrode, wherein the first electrode has a top surface and a sidewall surface
102
Deposit a resistance variable layer and a second electrode material over the top surface and the sidewall surface of the first electrode
103
Etch a portion of the second electrode material and the resistance variable layer to form a second electrode over the sidewall surface of the first electrode
104
Form a conductive plug contacting the second electrode
105

FIG. 1

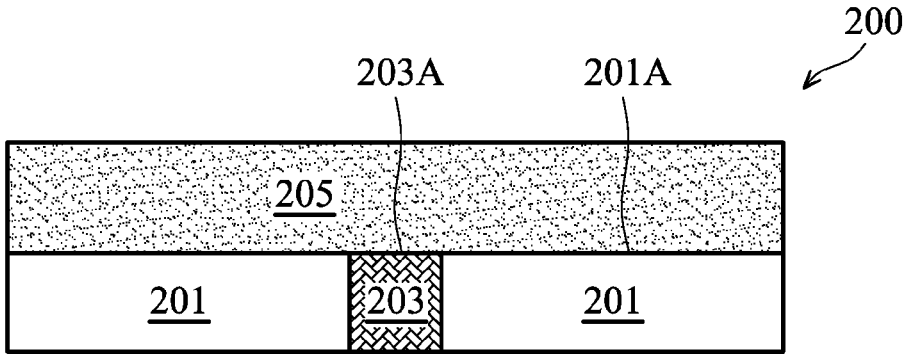
200
203A
201A
205
201
203
201

FIG. 2A

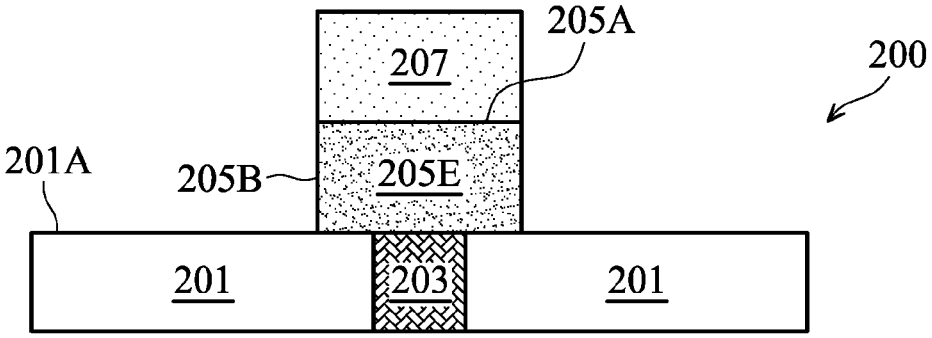
205A
207
200
201A
205B
205E
201
203
201

FIG. 2B

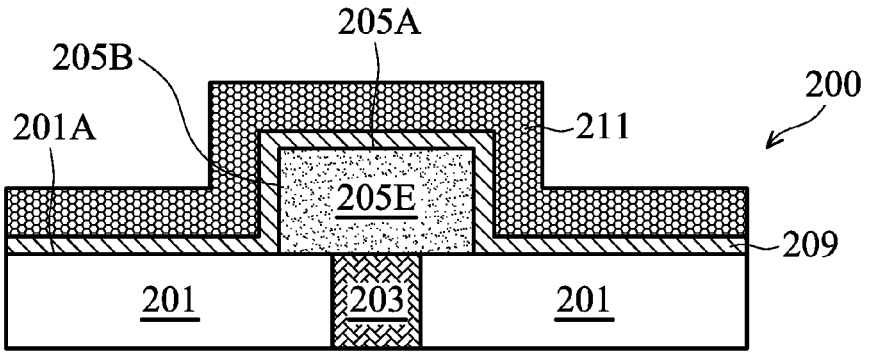
205A
205B
200
201A
211
205E
209
201
203
201

FIG. 2C

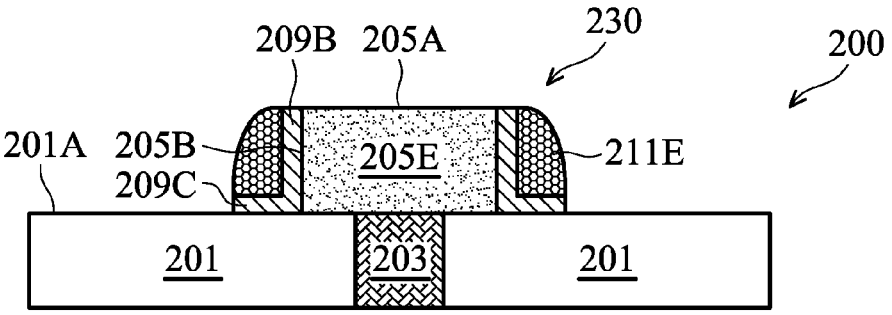
230
209B
205A
200
201A
205B
205E
211E
209C
201
203
201

FIG. 2D

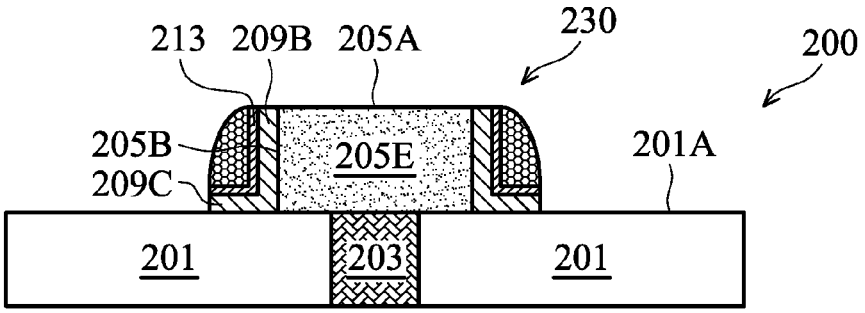
213
209B
205A
230
200
205B
205E
201A
209C
201
203
201

FIG. 2E

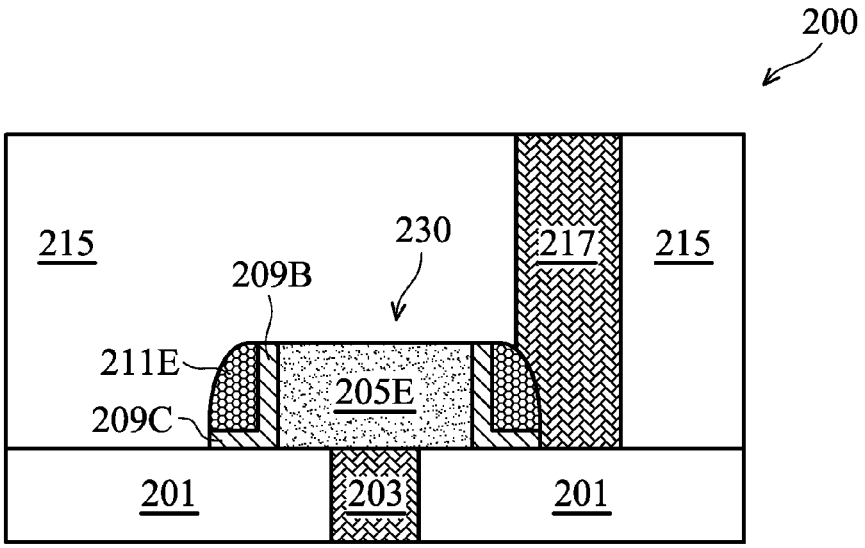
200
215
230
217
215
209B
211E
205E
209C
201
203
201

FIG. 2F

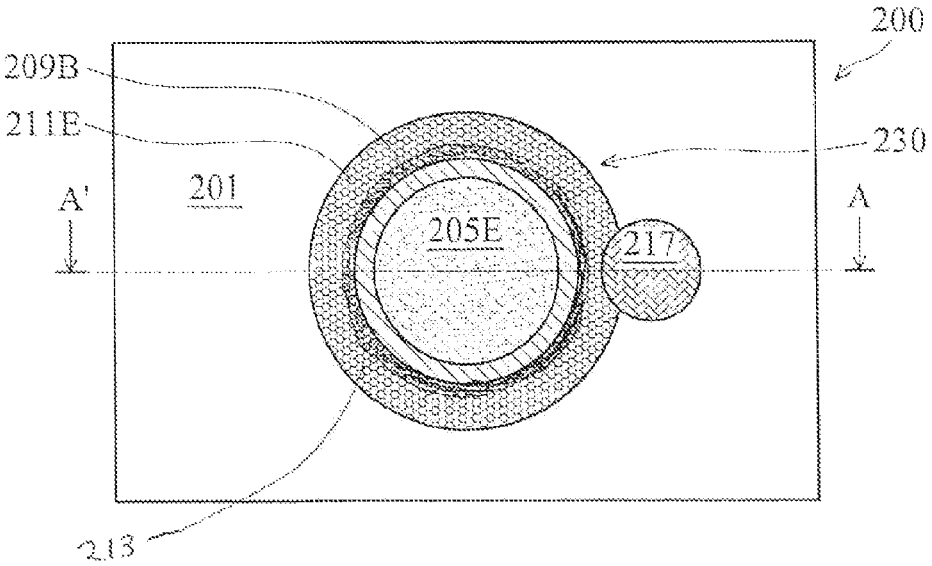
200
209B
211E
230
A'
201
205E
217
A
213

FIG. 2G

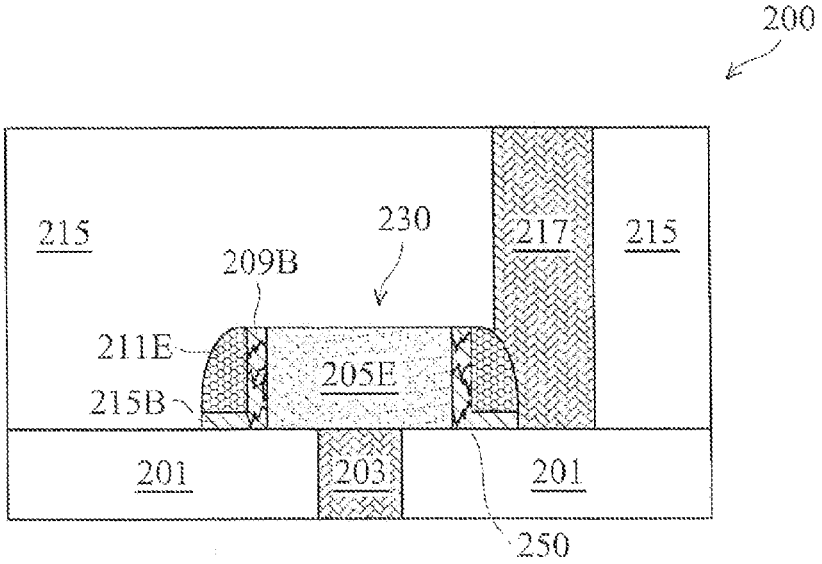
200
215
230
217
215
209B
211E
205E
215B
201
203
201
250

FIG. 2H

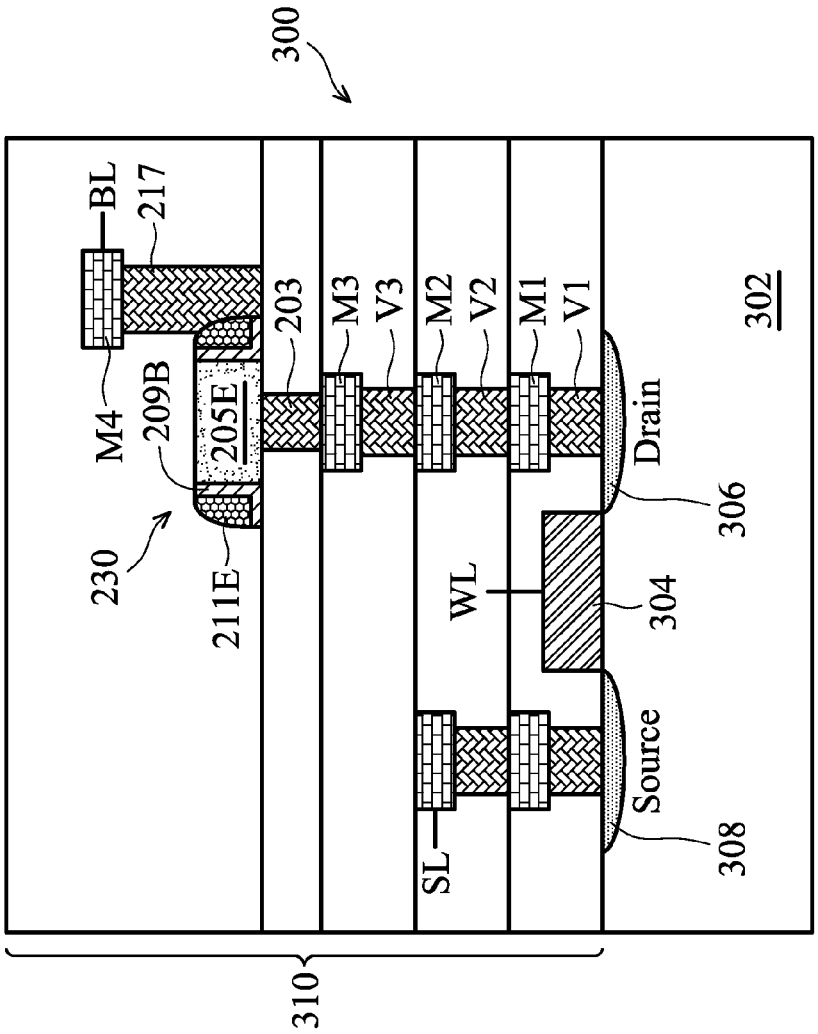
300
BL
217
M4
209B
205E
230
211E
203
M3
V3
M2
V2
M1
V1
WL
SL
Drain
Source
306
304
308
302
310

FIG. 3

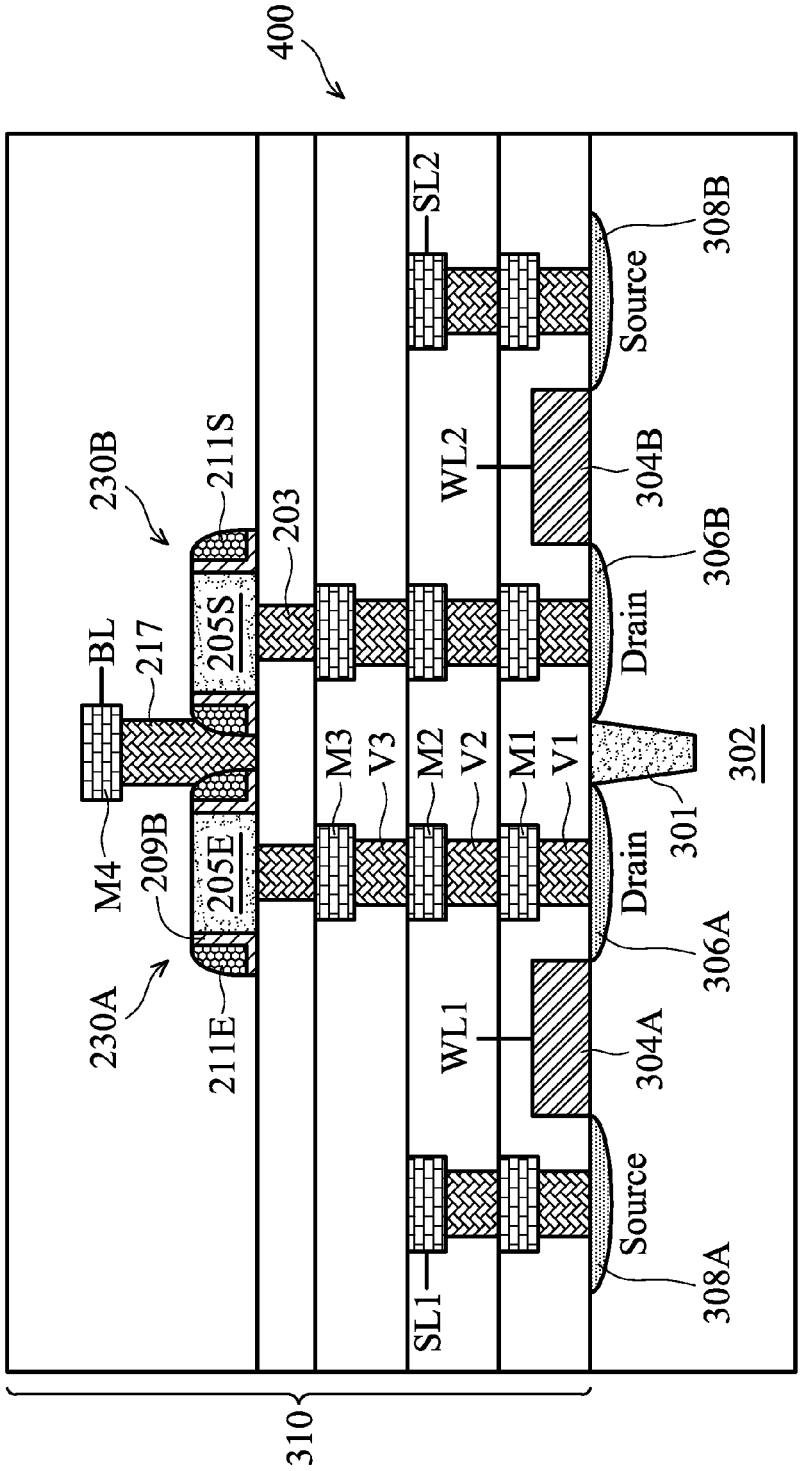
400
230B
211S
203
BL
217
205S
M4
209B
205E
230A
211E
M3
V3
M2
V2
M1
V1
SL2
WL2
WL1
SL1
Source
308B
304B
306B
Drain
302
301
Drain
306A
304A
Source
308A
310

FIG. 4

# RESISTANCE VARIABLE MEMORY STRUCTURE AND METHOD OF FORMING THE SAME

## TECHNICAL FIELD

This disclosure relates generally to a semiconductor structure and, more particularly, to a resistance variable memory structure and method of forming a resistance variable memory structure.

## BACKGROUND

In integrated circuit (IC) devices, resistive random access memory (RRAM) is an emerging technology for next generation non-volatile memory devices. RRAM is a memory structure including an array of RRAM cells each stores a bit of data using resistance, rather than electronic charge. Particularly, each RRAM cell includes a resistance variable layer, the resistance of which can be adjusted to represent logic "0" or logic "1".

From an application point of view, RRAM has many advantages. RRAM has a simple cell structure and CMOS logic comparable processes which result in a reduction of the manufacturing complexity and cost in comparison with other non-volatile memory structures. Despite the attractive properties noted above, a number of challenges exist in connection with developing RRAM. Various techniques directed at configurations and materials of these RRAMs have been implemented to try and further improve device performance.

## BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure may be understood from the following detailed description and the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flowchart of a method of forming a semiconductor structure having a resistance variable memory structure according to at least one embodiment of this disclosure.

FIGS. **2**A to **2**F are cross-sectional views of semiconductor structures having a resistance variable memory structure at various stages of manufacture according to one or more embodiments of the method of FIG. **1**.

FIG. **2**G is a planar view of the semiconductor structure having the resistance variable memory structure of FIG. **2**F.

FIG. **2**H is a cross-sectional view taken along line A-A' in FIG. **2**G to show the semiconductor structure in operation with filaments formed in the resistance variable layer according to one or more embodiments of this disclosure.

FIG. **3** is a cross-sectional view of a semiconductor structure having the resistance variable memory structure in FIG. **2**D (or **2**E) according to at least one embodiment of this disclosure.

FIG. **4** is a cross-sectional view of a semiconductor structure having the resistance variable memory structure in FIG. **2**D (or **2**E) according to some embodiments of this disclosure.

## DETAILED DESCRIPTION

The making and using of illustrative embodiments are discussed in detail below. It should be appreciated, however, that the disclosure provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts.



The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.

According to one or more embodiments of this disclosure, a semiconductor structure includes a resistance variable memory structure. The resistance variable memory structure includes a resistance variable layer formed between two electrodes. By applying a specific voltage to each of the two electrodes, an electric resistance of the resistance variable layer is altered. The low and high resistances are utilized to indicate a digital signal "1" or "0", thereby allowing for data storage. The switching behavior depends not only on the materials of the resistance variable layer but also on the choice of electrodes and interfacial properties of the electrodes.

According to one or more embodiments of this disclosure, the semiconductor structure having a resistance variable memory structure is formed within a chip region of a substrate. A plurality of semiconductor chip regions is marked on the substrate by scribe lines between the chip regions. The substrate will go through a variety of cleaning, layering, patterning, etching and doping steps to form the semiconductor structures. The term "substrate" herein generally refers to a bulk substrate on which various layers and device structures are formed. In some embodiments, the bulk substrate includes silicon or a compound semiconductor, such as GaAs, InP, Si/Ge, or SiC. Examples of the layers include dielectric layers, doped layers, polysilicon layers or conductive layers. Examples of the device structures include transistors, resistors, and/or capacitors, which may be interconnected through an interconnect layer to additional integrated circuits.

FIG. **1** is a flowchart of a method **100** of forming a semiconductor structure having a resistance variable memory structure according to at least one embodiment of this disclosure. FIGS. **2**A to **2**F are cross-sectional views of a semiconductor structure **200** having a resistance variable memory structure at various stages of manufacture according to various embodiments of the method **100** of FIG. **1**. Additional processes may be performed before, during, or after the method **100** of FIG. **1**. Various figures have been simplified for a better understanding of the inventive concepts of the present disclosure.

Referring now to FIG. **1**, the flowchart of the method **100** begins with operation **101**. In at least one embodiment, a dielectric layer is formed over a substrate. At least one conductive structure is formed over the substrate and embedded in the dielectric layer. The at least one conductive structure has a portion exposed to a top surface of the dielectric layer. A first electrode material is deposited over the conductive structure and the dielectric layer.

Referring to FIG. **2**A, which is a cross-sectional view of a portion of a semiconductor structure **200** having a resistance variable memory structure after performing operation **101**. The semiconductor structure **200** includes a substrate (not shown). In the illustrated examples of FIGS. **2**A-**2**F, the semiconductor structures **200** include a dielectric layer **201** formed on a top surface of the substrate (not shown). In at least one embodiment, the dielectric layer **201** includes one or more dielectric layers. The dielectric layer **201** comprises silicon oxide, fluorinated silica glass (FSG), carbon doped silicon oxide, silicon nitride, silicon oxynitride, tetra-ethyl-ortho-silicate (TEOS) oxide, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), BLACK DIAMOND® (Applied Materials of Santa Clara, Calif.), amorphous fluorinated carbon, low dielectric constant (low-k) dielectric material, or combinations thereof. The deposition process may

include chemical vapor deposition (CVD), atomic layer deposition (ALD), high density plasma CVD (HDPCVD) or spinning on glass.

A conductive structure **203** is formed embedded in the dielectric layer **201**. In certain embodiments, the conductive structure **203** includes a conductive interconnect, a doped region or a silicide region. In some embodiments, the conductive structure **203** includes aluminum, aluminum alloy, copper, copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, metal silicide, silicon or combinations thereof. In the illustrated example of FIG. **2**A, the semiconductor structure **200** may be formed by lithography patterning and etching in the dielectric layer **201**. A layer of the conductive structure **203** is deposited over the patterned dielectric layer **201** and subsequently planarized to form the conductive structure **203**. A top surface **203**A of the conductive structure **203** is substantially coplanar with a top surface **201**A the dielectric layer **201**.

A first electrode material **205** is deposited over top surfaces (**203**A and **201**A) of the conductive structure **203** and the dielectric layer **201**. The first electrode material **205** includes a conductive material having a proper work function such that a high work function wall is built between the first electrode material **205** and a resistance variable layer subsequently formed. The first electrode material **205** may comprise Pt, AlCu, TiN, Au, Ti, Ta, TaN, W, WN, Cu or combinations thereof. Possible formation methods include electroless plating, sputtering, electro plating, PVD or ALD. In some embodiments, the first electrode material **205** is electrically connected to an underlying electrical component, such as a transistor, through the conductive structure **203**.

Referring back to FIG. **1**, method **100** continues with operation **102**. In operation **102**, the first electrode material is patterned to form a first electrode. The first electrode has a top surface and a sidewall surface.

Referring to FIG. **2**B, which is a cross-sectional view of a portion of the semiconductor structure **200** after performing operation **102**. A mask layer **207** having a feature is formed over the first electrode material **205** and also over the conductive structure **203**. The feature is formed by a suitable process, including deposition, lithography patterning, and/or etching processes. An etching process is performed to remove the first electrode material **205** not underlying the feature of the mask layer **207**. Then, a first electrode **205**E is formed and contacts the conductive structure **203**.

The mask layer **207** is removed after the etching process from the semiconductor structure **200** and a top surface **205**A of the first electrode **205**E is exposed. Also, the first electrode **205**E has a sidewall surface **205**B connected to the top surface **205**A. The removing process of the mask layer **207** may include a dry etching process, wet etching process, or combination thereof.

Referring back to FIG. **1**, method **100** continues with operation **103**. In operation **103**, a resistance variable layer and a second electrode material are deposited over the top surface and the sidewall surface of the first electrode.

FIG. **2**C is a cross-sectional view of the semiconductor structure **200** after performing operation **103**. A resistance variable layer **209** is conformally deposited over the top surface **205**A and the sidewall surface **205**B of the first electrode **205**E, and the top surface **201**A of the dielectric layer **201**. The resistance variable layer **209** has a resistivity (or conductivity) capable of switching between a high resistance state and a low resistance state, by application of an electrical voltage. In various embodiments, the resistance variable layer **209** includes at least one of dielectric materials comprising a high dielectric constant (high-k) dielectric material, a binary metal oxide or a transition metal oxide. In some embodiments, the resistance variable layer **209** includes nickel oxide, titanium oxide, hafnium oxide, zirconium oxide, zinc oxide, tungsten oxide, aluminum oxide, tantalum oxide, molybdenum oxide or copper oxide. Possible formation methods include pulse laser deposition (PLD) or ALD, such as ALD with a precursor containing zirconium and oxygen. In one example, the resistance variable layer **209** has a thickness in a range from about 10 angstrom to about 500 angstrom.

A second electrode material **211** is conformally deposited over the resistance variable layer **209**. The second electrode material **211** may include suitable conductive material to electrically connect a subsequently formed resistance variable memory structure to other portions of an interconnect structure for electrical routing. The second electrode material **211** may comprise Pt, AlCu, TiN, Au, Ti, Ta, TaN, W, WN, Cu or combinations thereof. In at least one example, the second electrode material **211** has a thickness in a range from about **30** angstrom to about **3000** angstrom. In some embodiments, the first electrode material **205** and the second electrode material **211** have a same composition. In some embodiments, the first electrode material **205** and the second electrode material **211** have different compositions. Possible formation methods include electroless plating, sputtering, electro plating, PVD or ALD.

Referring back to FIG. **1**, the method **100** continues with operation **104** in which a portion of the second electrode material and the resistance variable layer are etched to form a second electrode over a sidewall of the first electrode.

FIG. **2**D is a cross-sectional view of the semiconductor structure **200** after performing operation **104**. In at least one embodiment, a portion of the second electrode material **211** and the resistance variable layer **209** are anisotropically etched to form a spacer over the sidewall **205**B of the first electrode **205**E without lithography patterning process. The spacer includes a vertical portion **209**B of a remaining resistance variable layer **209** over sidewall **205**B of the first electrode **205**E and a horizontal portion **209**C of the remaining resistance variable layer **209** over the top surface **201**A of the dielectric layer **201**. The spacer further includes a second electrode **211**E of the second electrode material **211** formed over the vertical portion **209**B and the horizontal portion **209**C of the remaining resistance variable layer **209**. A resistance variable memory structure **230** including the first electrode **205**E, the vertical portion **209**B and the horizontal portion **209**C of the resistance variable layer **209**, and the second electrode **211**E is formed.

In some examples, the semiconductor structure **200** further includes a cap layer **213** optionally formed between the remaining resistance variable layer **209** and the second electrode **211**E, such as over the vertical portion **209**B and the horizontal portion **209**C of the resistance variable layer **209** and underlying the second electrode **211**E as shown in FIG. **2**E. In some embodiments, the cap layer **213** includes a conductive material that is capable of depriving oxygen from the resistance variable layer **209** and thus causing vacancy defects formed in the resistance variable layer **209**. The cap layer **213** comprises titanium, tantalum or hafnium in some embodiments.

Referring back to FIG. **1**, the method **100** optionally continues with operation **105** in which a conductive plug is formed contacting the second electrode.

FIG. **2**F is a cross-sectional view of the semiconductor structure **200** after performing operation **105**. An inter-level dielectric (ILD) layer **215** may be blanket formed over the resistance variable memory structure **230**. A chemical mechanical polishing (CMP) process is further applied to the

semiconductor structure **200** to planarize the ILD layer **215**. The ILD layer **215** may include multiple dielectric layers. The ILD layer **215** may comprise silicon oxide, fluorinated silica glass (FSG), carbon doped silicon oxide, silicon nitride, silicon oxynitride, TEOS oxide, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), amorphous fluorinated carbon, low-k dielectric material, or combinations thereof.

An opening is etched in the ILD layer **215** to expose a portion of the second electrode **211**E. A conductive material of a contact plug **217** may overfill the opening in the ILD layer **215**. The conductive material may include copper, copper alloys, aluminum or tungsten. The possible formation methods include electroless plating, sputtering, electro plating or chemical vapor deposition (CVD). The excess conductive material outside of the opening is removed through a suitable process such as chemical mechanical polishing (CMP). The contact plug **217** having the conductive material is formed contacting the second electrode **211**E of the resistance variable memory structure **230**.

FIG. **2**G is a planar view of the semiconductor structure **200**. FIG. **2**F is the cross-sectional view obtained from a vertical plane crossing line A-A' in FIG. **2**G. In FIG. **2**G, the first electrode **205**E is surrounded by the vertical portion **209**B of the resistance variable layer **209**. The vertical portion **209**B of the resistance variable layer **209** is surrounded by the second electrode **211**E. The vertical portion **209**B of the resistance variable layer **209** and the second electrode **211**E are closed loops surrounding the first electrode **205**E. When the semiconductor structure **200** is cut through crossing line A-A' in FIG. **2**G, the second electrode **21 1**E is illustrated as two portions on opposite sides of the first electrode **205**E in FIG. **2**F. The conductive structure **203** in FIG. **2**F and the horizontal portion **209**C of the resistance variable layer **209** in FIG. **2**F are underlying the first electrode **205**E and the second electrode **21 1**E, respectively. Hence, the conductive structure **203** and the horizontal portion **209**C in FIG. **2**F are not shown in FIG. **2**G.

FIG. **2**H is a cross-sectional view of the semiconductor structure **200** having a resistance variable memory structure in various operations for data storage.

In a "forming" operation, a "forming" voltage is applied to the first and second electrodes **205**E and **211**E of the resistance variable memory structure **230**. The "forming" voltage is high enough to generate a conductive portion in the vertical portion **209**B of the resistance variable layer **209**. In one example, the conductive portion includes one or more conductive filaments **250** to provide a conductive path such that the vertical portion **209**B of the resistance variable layer **209** shows an "on" or low resistance state. The conductive path may be related to the lineup of the defect (e.g. oxygen) vacancies in the vertical portion **209**B of the resistance variable layer **209**. In some embodiments, the "forming" voltage is applied only one time. Once the conductive path is formed, the conductive path will remain present in the resistance variable layer **209**B. Other operations may disconnect or reconnect the conductive path using smaller voltages or different voltages.

In a "reset" operation, a "reset" voltage high enough to break the conductive path in the resistance variable layer **209**B is applied to the resistance variable memory structure **230** such that the resistance variable layer **209**B shows an "off" or high resistance state.

In a "set" operation, a "set" voltage high enough to reconnect the conductive path in the resistance variable layer **209**B is applied to the resistance variable memory structure **230** such that the resistance variable layer **209**B shows the "on" or low resistance state. The "set" operation turns the resistance variable layer **209**B to the low resistance state. By applying a specific voltage between two electrodes **205**E and **211**E, an electric resistance of the resistance variable layer **209**B is altered after applying the specific voltage. The low and high resistances are utilized to indicate a digital signal "1" or "0", thereby allowing for data storage.

FIG. **3** shows a cross-sectional view of a semiconductor structure **300** with the resistance variable memory structure **230** of FIG. **2**D (or **2**E) according to at least one embodiment of the present disclosure. The semiconductor structure **300** may be formed on a substrate **302** such as silicon, germanium, and/or a compound semiconductor material. The semiconductor structure **300** may include an access transistor that includes as a gate electrode **304**, a drain region **306** and a source region **308** on opposite sides of the gate electrode **304**. The gate electrode **304** is formed on a top surface of the substrate **302**. The source region **308** and the drain region **306** are formed by implantation in a portion of the substrate **302**. Multiple dielectric layers **310** are formed over the access transistor and the substrate **302**. Details of the materials and fabrication methods of the multiple dielectric layers **310** can be found in the text associated with the dielectric layer **201** in the semiconductor structure **200** and are not repeated here.

Referring still to FIG. **3**, a plurality of stacked metallization layers and via layers are formed over the access transistor and embedded in the dielectric layers **310**. In at least one embodiment, the plurality of metallization layers includes four metal layers M**1** to M**4**. Vertical columnar vias (V**1** to V**3**, **203** and **217**) interconnect the source region **232** and the drain region **231** to metallization layer M**1**, and connect different metallization layers M**1**, M**2**, M**3**, and M**4**. The plurality of stacked metal features and via layers provides interconnections between devices structures, circuits and/or inputs/outputs terminals. The metallization layers and via layers may include aluminum, aluminum alloy, copper, copper alloy, titanium, titanium nitride, tantalum, tantalum nitride, tungsten, metal silicide, or combinations thereof.

In some embodiments, there are at least three metallization layers overlying the access transistor and underlying the resistance variable memory structure **230**. In this illustrated example, the resistance variable memory structure **230** is formed between metallization layers M**3** and M**4**. Vertical columnar vias **203** and **217** electrically connect the resistance variable memory structure **230** to the metallization layers M**3** and M**4**, respectively. The source region **308** of the access transistor is coupled to a source line SL in metallization layer M**2** through columnar via V**1**, metallization layer M**1** and columnar via V**2**. A word line WL is electrically coupled to the gate electrode **304** to provide a gate voltage to turn on the access transistor. The drain region **306** may be coupled to the first electrode **205**E of the resistance variable memory structure **230** through columnar vias (V**1** to V**3** and **203**) and metallization layers (M**1** to M**3**). A bit line BL in metallization layer M**4** is electrically coupled to the second electrode **211**E of the resistance variable memory structure **230** through the columnar via **217**.

Generally, some of the processes for forming the bottom metallization layers (M**1** to M**3**) may have a process temperature higher than 400° C., such as the processes for annealing or dielectric layer formation. The stability of a resistance variable memory structure **230** may be affected by the high temperature processes if the resistance variable memory structure **230** is formed before the high temperature processes. In this embodiment, the resistance variable memory structure **230** is formed over the bottom metallization layers (M**1** to M**3**). This disclosure eliminates the drawbacks of high temperature effect on the resistance variable memory struc-

ture **230** in bottom metallization layers (M**1** to M**3**). Furthermore, there are several control lines (such as the source line, the word line and the bit line) used to control the operation of the resistance variable memory structure **230** and the access transistor. There are many spaces needed in bottom metallization layers for circuit routing to arrange these control lines. Advantageously, the resistance variable memory structure **230** is formed over the bottom metallization layers (M**1** to M**3**). In this illustrated example, the resistance variable memory structure **230** is formed between metallization layers M**3** and M**4**. In accordance with one or more embodiments of the present disclosure, there are more spaces for circuit routing by forming the resistance variable memory structure **230** in the upper metallization layers.

FIG. **4** shows a semiconductor structure **400** substantially similar to the semiconductor structure **300** disclosed in FIG. **3**. The description of the common structures are not repeated here although fully applicable in the following embodiments as well.

The semiconductor structure **400** having two resistance variable memory structures **230**A and **230**B substantially similar to the resistance variable memory structure **230** of FIG. **2**D (or **2**E). Second electrodes **211**E and **211**S of the resistance variable memory structures **230**A and **230**B contact (or share) a same columnar via **217**. Through the columnar via **217**, a bit line BL in metallization layer M**4** is electrically coupled to the second electrode **211**E of the resistance variable memory structure **230**A and the second electrode **211** S of the resistance variable memory structure **230**B. Advantageously, the resistance variable memory structures **230**A and **230**B shared the same columnar via **217** provides extra space for functional integrated circuits and circuit routing.

The semiconductor structure **400** includes a first access transistor having a gate electrode **304**A, a drain region **306**A and a source region **308**A on opposite sides of the gate electrode **304**A. The semiconductor structure **400** also includes a second access transistor having a gate electrode **304**B, a drain region **306**B and a source region **308**B on opposite sides of the gate electrode **304**B. The first access transistor and the second access transistor are isolated by a shallow trench isolation (STI) structure **301** formed by dielectric materials. Multiple dielectric layers **310** are formed over the access transistors and the substrate **302**.

Referring still to FIG. **4**, a plurality of stacked metallization layers (M**1** to M**4**) and via layers (V**1** to V**3**, **203** and **217**) are formed over the access transistors and embedded in the dielectric layers **310**. The plurality of stacked metal features and via layers provides interconnections between the access transistors, the resistance variable memory structures (**230**A and **230**B), circuits and/or inputs/outputs terminals.

During various operations of the resistance variable memory structure **230**A, a source line SL**1** in metallization layer M**2** electrically coupled to the source region **308**A of the first access transistor provides a source voltage. A bit line BL in metallization layer M**4** electrically coupled to the drain region **306**A of the first access transistor provides a drain voltage. A word line WL**1** electrically coupled to the gate electrode **304**A of the first access transistor is turned on with a gate voltage. The resistance variable memory structure **230**A is able to perform previous mentioned "forming", "set" and "reset" operations for data storage. During various operations of the resistance variable memory structure **230**A, the gate electrode **304**B of the second access transistor is turned off and the source region **308**B is floating.

Likewise, the resistance variable memory structure **230**B is able to perform previous mentioned "forming", "set" and "reset" operations for data storage by applying specific voltages to the source region **308**B (through a source line SL**2** in metallization layer M**2**), the drain region **306**B (through the same bit line BL in metallization layer M**4**) and the gate electrode **304**B (through a word line WL**2**) of the second access transistor. During various operations of the resistance variable memory structure **230**B, the gate electrode **304**A of the first access transistor is turned off and the source region **308**A is floating.

In some embodiments, the source line SL**1** and the source line SL**2** is a same source line. The resistance variable memory structures **230**A and **230**B share a same source line for the respective access transistors to provide extra space for functional integrated circuits and circuit routing. In certain embodiments, the source line SL**1** and the source line SL**2** have different source lines for circuit design concern.

In FIG. **4**, the resistance variable memory structures (**230**A and **230**B) and the shared columnar via **217** are formed overlying three metallization layers (M**1** to M**3**). However, this disclosure is not limited to the above conditions for forming the resistance variable memory structures (**230**A and **230**B) and the shared columnar via **217** above at least three metallization layers, and differing conditions that produce the above shared columnar via for at least two resistance variable memory structures are within the scope of this disclosure.

Various embodiments of the present disclosure may be used to improve the processes of a resistance variable memory structure. For example, the disclosed method **100** includes a single lithography patterning process in forming the first electrode **205**E in operation **102**. The second electrode **211**E is formed by a spacer etching process without lithography patterning process in operation **104**. The disclosed method **100** includes a single lithography patterning process (in operation **102**) used to form both electrodes **205**E and **211**E. This disclosure eliminates drawbacks in other methods which use multiple lithography patterning process steps in patterning both the first and second electrodes. The manufacturing complexity and cost are reduced in accordance with some embodiments.

One aspect of the disclosure describes a semiconductor structure including a resistance variable memory structure. The semiconductor structure also includes at least three metallization layers over a substrate. A dielectric layer is over the at least three metallization layers. The resistance variable memory structure is over the dielectric layer. The resistance variable memory structure includes a first electrode disposed over the dielectric layer. The first electrode has a sidewall surface. A resistance variable layer has a first portion over the sidewall surface of the first electrode, and a second portion extending from the first portion away from the first electrode. A second electrode is over the resistance variable layer.

A further aspect of the disclosure describes a semiconductor structure including a resistance variable memory structure. The semiconductor structure also includes an access transistor. The access transistor includes a source region and a drain region on opposite sides of a gate electrode. At least three metallization layers are over the access transistor. The resistance variable memory structure is over the at least three metallization layers. The resistance variable memory structure includes a first electrode disposed over the conductive structure. The first electrode has a sidewall surface. A resistance variable layer has a vertical portion and a horizontal portion. The vertical portion surrounds the sidewall surface of the first electrode and the horizontal portion extends from the vertical portion away from the first electrode. A second electrode is over the resistance variable layer and surrounds the vertical portion of the resistance variable layer.

Another aspect of the disclosure describes a semiconductor structure including resistance variable memory structures. The semiconductor structure also includes a substrate. A first resistance variable memory structure adjacent to a second resistance variable memory structure disposed over the substrate. Each resistance variable memory structure includes a first electrode, a resistance variable layer and a second electrode. The first electrode is disposed over the substrate and has a sidewall surface. The resistance variable layer has a first portion over the sidewall surface of the first electrode, and a second portion extending from the first portion away from the first electrode. The second electrode is over the resistance variable layer. A contact plug contacts both second electrodes of the first and second resistance variable memory structures.

Although the embodiments and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. As one of ordinary skill in the art will readily appreciate from the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed:

**1**. A semiconductor structure, comprising:

at least three metallization layers over a substrate;

a dielectric layer over the at least three metallization layers; and

a resistance variable memory structure over the dielectric layer, the resistance variable memory structure comprising:

a first electrode disposed over the dielectric layer, the first electrode having a sidewall surface;

a resistance variable layer having a first portion which is a closed loop and surrounds the sidewall surface of the first electrode and a second portion which extends from the first portion away from the first electrode;

a second electrode disposed over the resistance variable layer; and

a conductive cap layer disposed between the resistance variable layer and the second electrode a conductive plug contacting the second electrode and the resistance variable layer.

**2**. The semiconductor structure of claim **1**, wherein the conductive cap layer comprises titanium, tantalum or hafnium.

**3**. The semiconductor structure of claim **1**, further comprising a conductive structure embedded in the dielectric layer, and electrically connected to the first electrode and the at least three metallization layers.

**4**. The semiconductor structure of claim **1**, wherein each of the first electrode and the second electrode comprises at least one selected from the group consisting of Pt, AlCu, TiN, Au, Ti, Ta, TaN, W, WN, and Cu.

**5**. The semiconductor structure of claim **1**, wherein the resistance variable layer comprises a high-k dielectric material, a binary metal oxide or a transition metal oxide.

**6**. The semiconductor structure of claim **1** further comprising an access transistor having a source region and a drain region underlying the at least three metallization layer, wherein the first electrode is electrically connected to the drain region of the access transistor.

**7**. The semiconductor structure of claim **1**, wherein the second electrode is a closed loop surrounding the resistance variable layer and the first electrode.

**8**. The semiconductor structure of claim **1**, wherein the second portion is a portion of the closed loop and surrounds the first electrode.

**9**. The semiconductor structure of claim **1**, wherein the second portion of the resistance variable layer is disposed between the second electrode and the dielectric layer.

**10**. The semiconductor structure of claim **9**, wherein the first portion is selectively configurable to form at least one conductive path between the first electrode and the second electrode.

**11**. A semiconductor structure, comprising:

an access transistor comprising a source region and a drain region on opposite sides of a gate electrode;

at least three metallization layer over the access transistor; and

a resistance variable memory structure over the at least three metallization layer, the resistance variable memory structure comprising:

a first electrode disposed over the at least three metallization layer, wherein the first electrode is electrically connected to the drain region of the access transistor and has a sidewall surface;

a resistance variable layer having a vertical portion and a horizontal portion, wherein the vertical portion is a closed loop and surrounds the sidewall surface of the first electrode and the horizontal portion extends from the vertical portion away from the first electrode;

a second electrode disposed over the resistance variable layer and surrounding the vertical portion of the resistance variable layer; and

a conductive cap layer disposed between the resistance variable layer and the second electrode a conductive plug contacting the second electrode and the resistance variable layer.

**12**. The semiconductor structure of claim **11**, wherein the vertical portion is selectively configurable to form at least one conductive path between the first electrode and the second electrode.

**13**. The semiconductor structure of claim **11**, wherein the resistance variable layer comprises a high-K dielectric material, a binary metal oxide or a transition metal oxide.

**14**. The semiconductor structure of claim **11**, wherein each of the first electrode and the second electrode comprises at least one selected from the group consisting of Pt, AlCu, TiN, Au, Ti, Ta, TaN, W, WN, and Cu.

**15**. The semiconductor structure of claim **11**, wherein the conductive cap layer surrounds the resistance variable layer.

**16**. A semiconductor structure, comprising:

a substrate;

a first resistance variable memory structure adjacent to a second resistance variable memory structure disposed over the substrate, each of the first and the second resistance variable memory structure comprising:

a first electrode disposed over the substrate and having a sidewall surface;

a resistance variable layer having a first portion which is a closed loop and surrounds the sidewall surface of the first electrode and a second portion which extends from the first portion away from the first electrode; and

a second electrode disposed over the resistance variable layer; and

a conductive plug contacting both second electrodes and resistance variable layers of the first and second resistance variable memory structures.

**17**. The semiconductor structure of claim **16** further comprising:

a first access transistor and a second access transistor underlying the first and second resistance variable memory structures, wherein each of the first and second access transistors has a source region and a drain region, wherein the drain region of each access transistor is electrically connected to the first electrode of the first and second resistance variable memory structures respectively.

**18**. The semiconductor structure of claim **17**, wherein the source region of each access transistor is configurable to connect a same source line.

**19**. The semiconductor structure of claim **16**, wherein the first portion is selectively configurable to form at least one conductive path between the first electrode and the second electrode.

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