



US009406843B2

(12) **United States Patent**
Aldaz et al.

(10) **Patent No.:** **US 9,406,843 B2**
(45) **Date of Patent:** ***Aug. 2, 2016**

(54) **METHODS AND DEVICES FOR LIGHT EXTRACTION FROM A GROUP III-NITRIDE VOLUMETRIC LED USING SURFACE AND SIDEWALL ROUGHENING**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/632,755**

(22) Filed: **Feb. 26, 2015**

(65) **Prior Publication Data**

US 2015/0207032 A1 Jul. 23, 2015

Related U.S. Application Data

(63) Continuation of application No. 13/781,633, filed on Feb. 28, 2013, now Pat. No. 9,000,466, which is a continuation-in-part of application No. 12/861,765, filed on Aug. 23, 2010, now abandoned.

(60) Provisional application No. 61/605,026, filed on Feb. 29, 2012.

(51) **Int. Cl.**
H01L 33/22 (2010.01)
H01L 33/20 (2010.01)
H01L 33/58 (2010.01)
H01L 33/32 (2010.01)
H01L 33/00 (2010.01)
H01L 33/18 (2010.01)

(52) **U.S. Cl.**
CPC **H01L 33/22** (2013.01); **H01L 33/0075** (2013.01); **H01L 33/18** (2013.01); **H01L 33/32** (2013.01); **H01L 33/58** (2013.01); **H01L 2933/0033** (2013.01); **H01L 2933/0083** (2013.01)

(58) **Field of Classification Search**
CPC H01L 33/22; H01L 33/20
USPC 257/98, 94, E33.001
See application file for complete search history.

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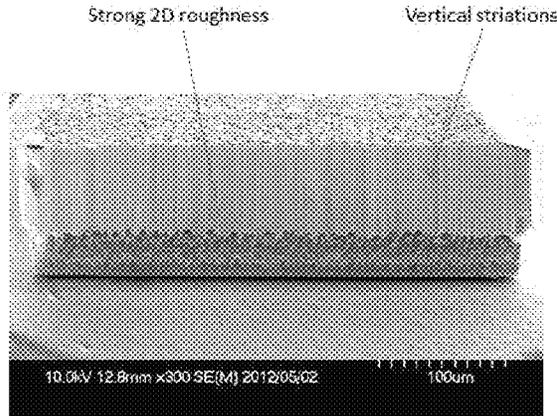
Primary Examiner — Marc Armand

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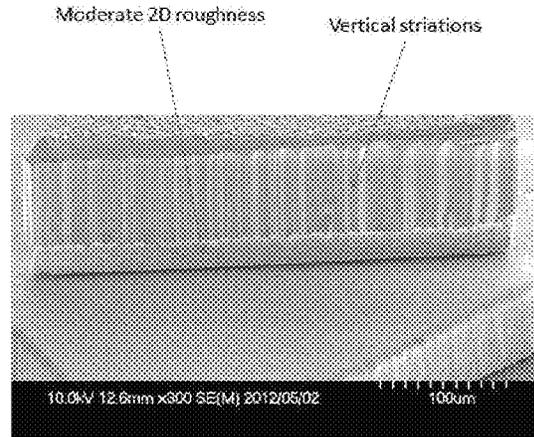
(57) **ABSTRACT**

Embodiments of the present disclosures are directed to improved approaches for achieving high-performance light extraction from a Group III-nitride volumetric LED chips. More particularly, disclosed herein are techniques for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening.

28 Claims, 24 Drawing Sheets



Method 1



Method 2

100 →

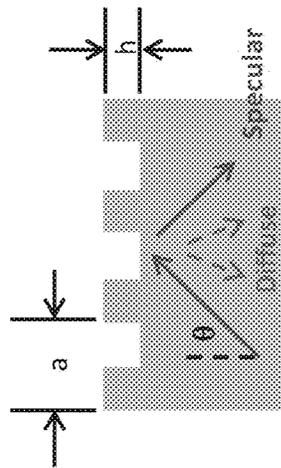
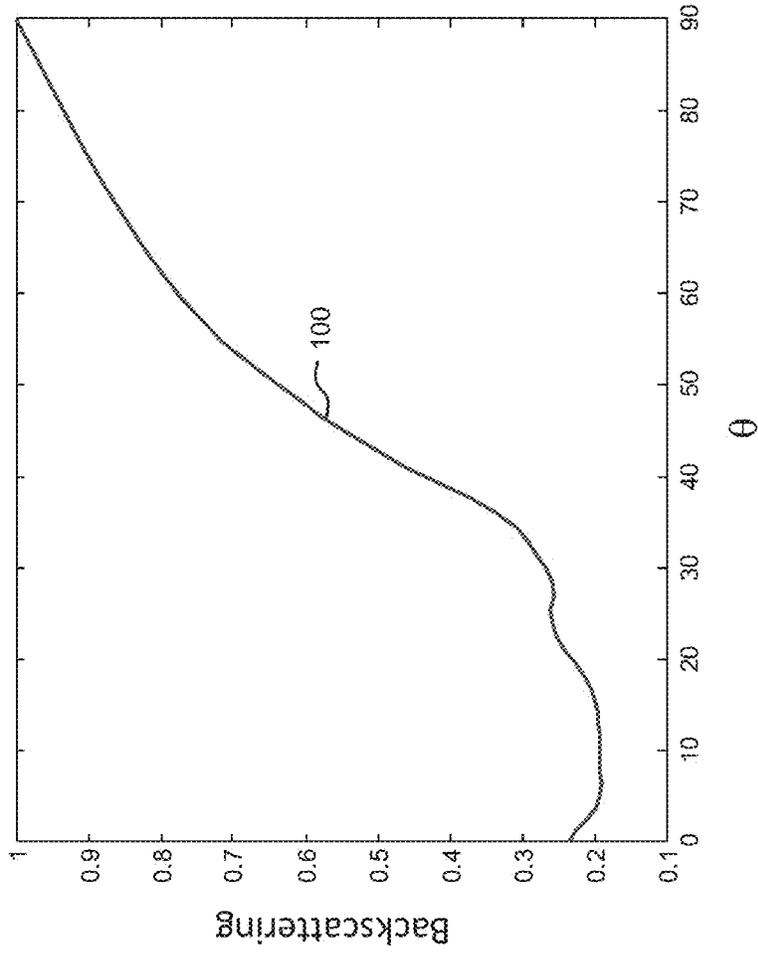


FIG. 1

200

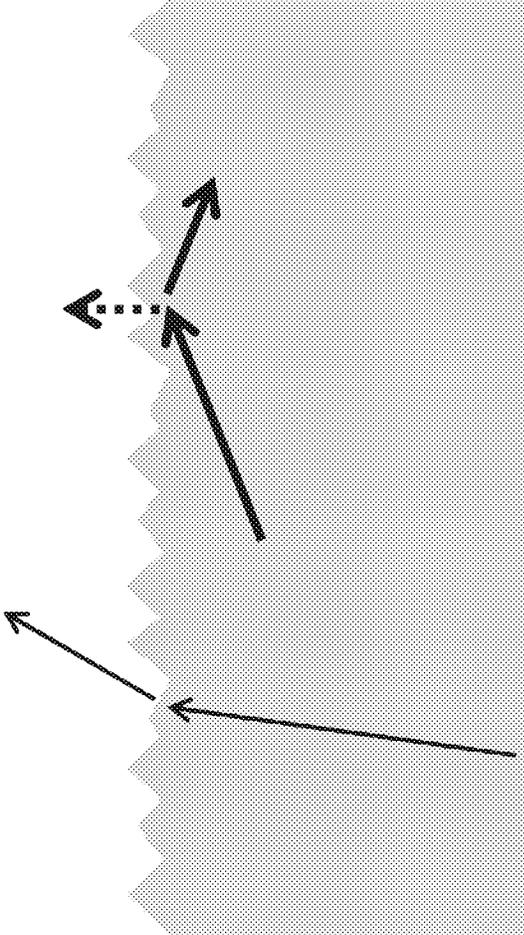


FIG. 2

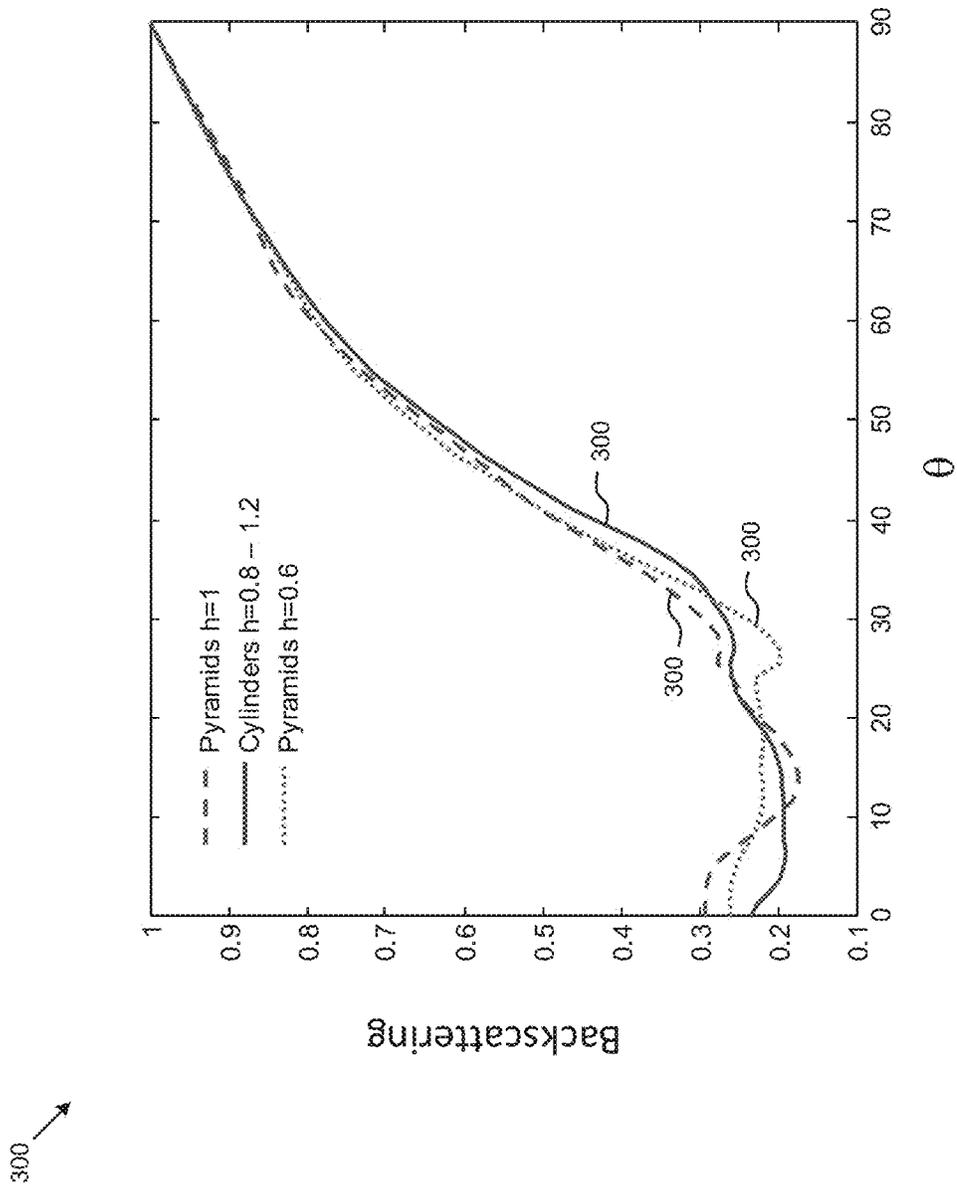


FIG. 3

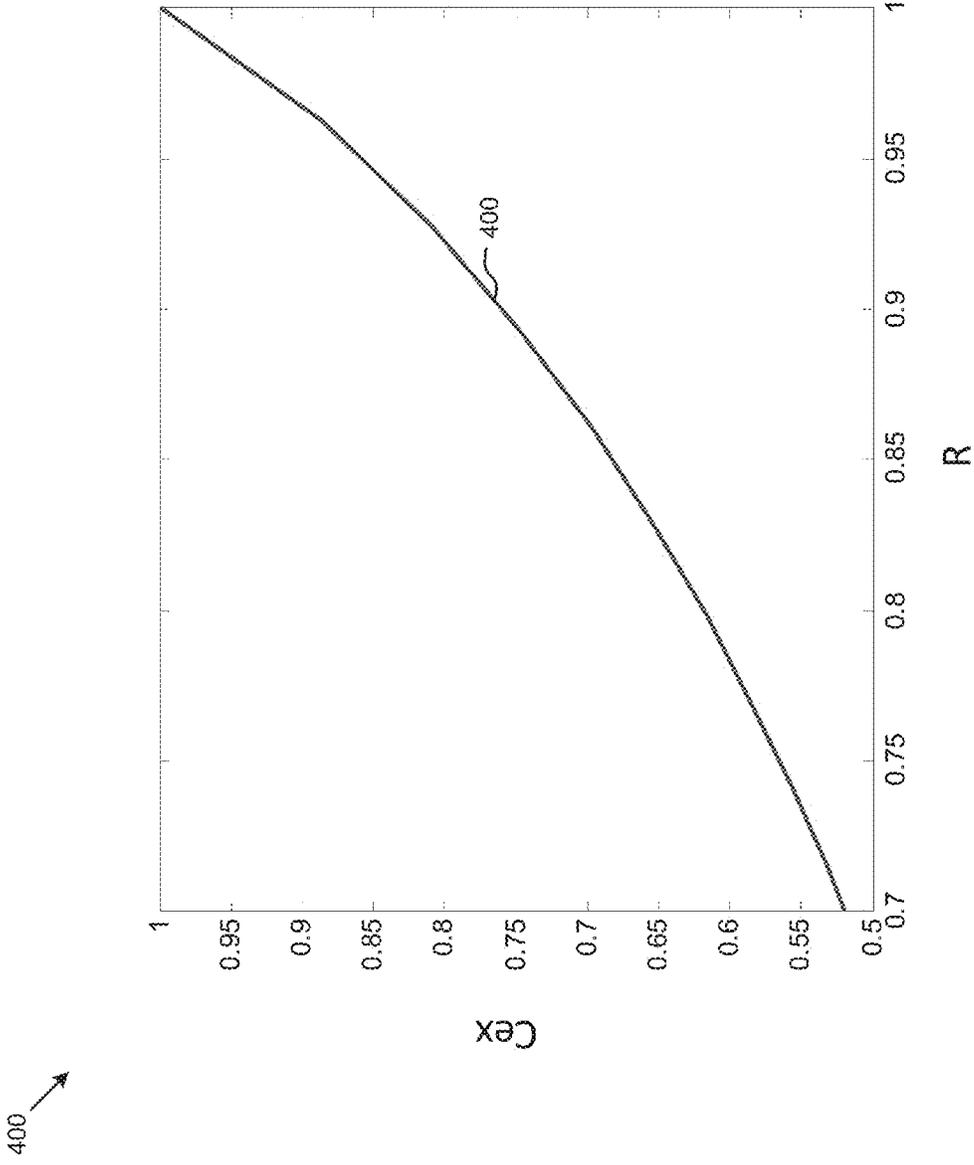


FIG. 4

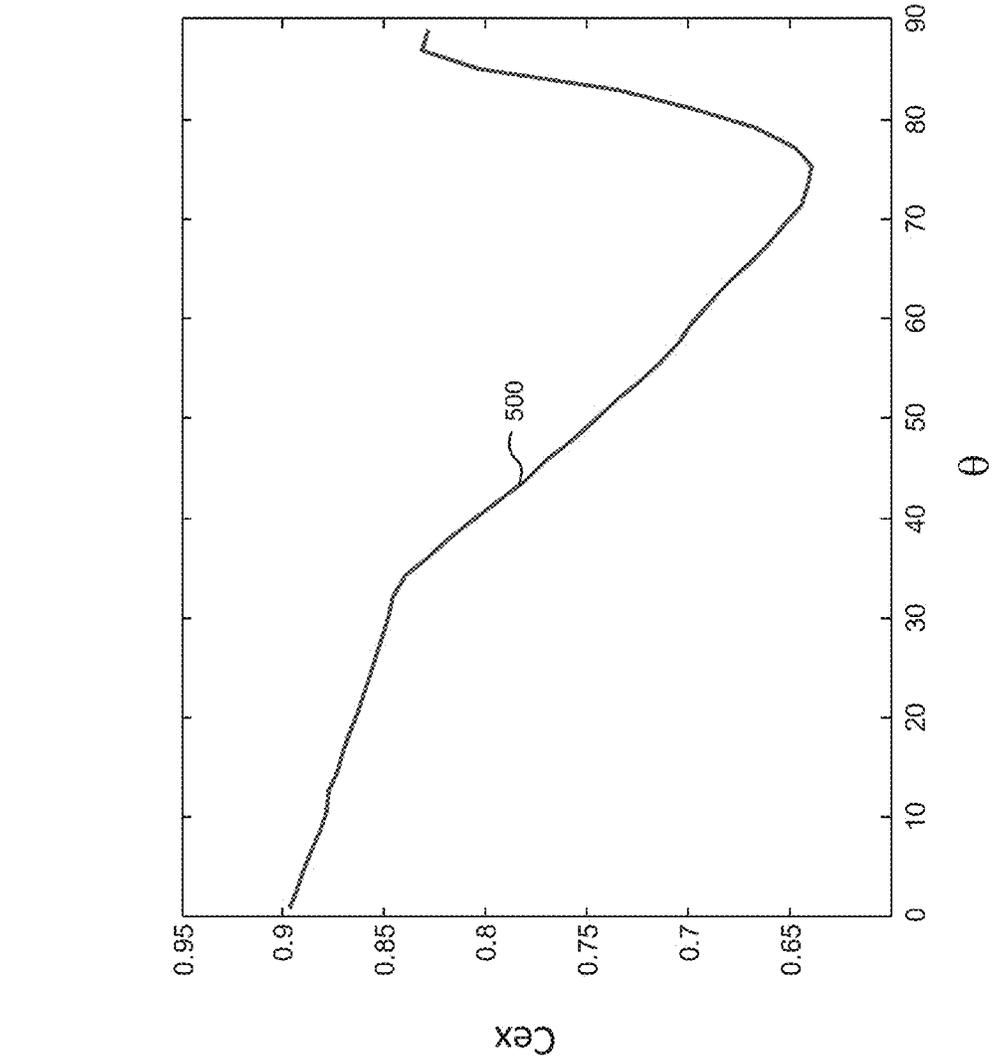


FIG. 5

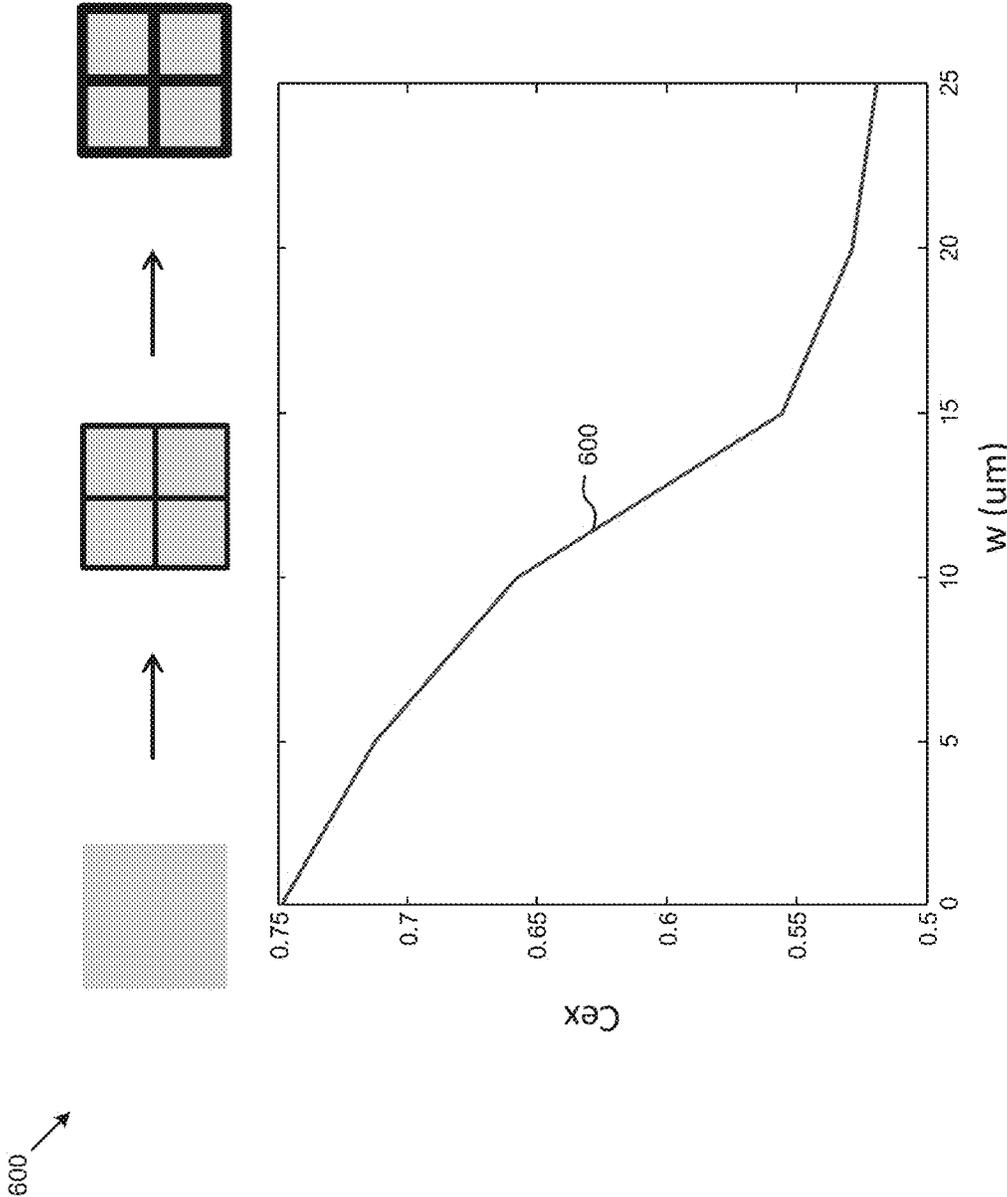


FIG. 6

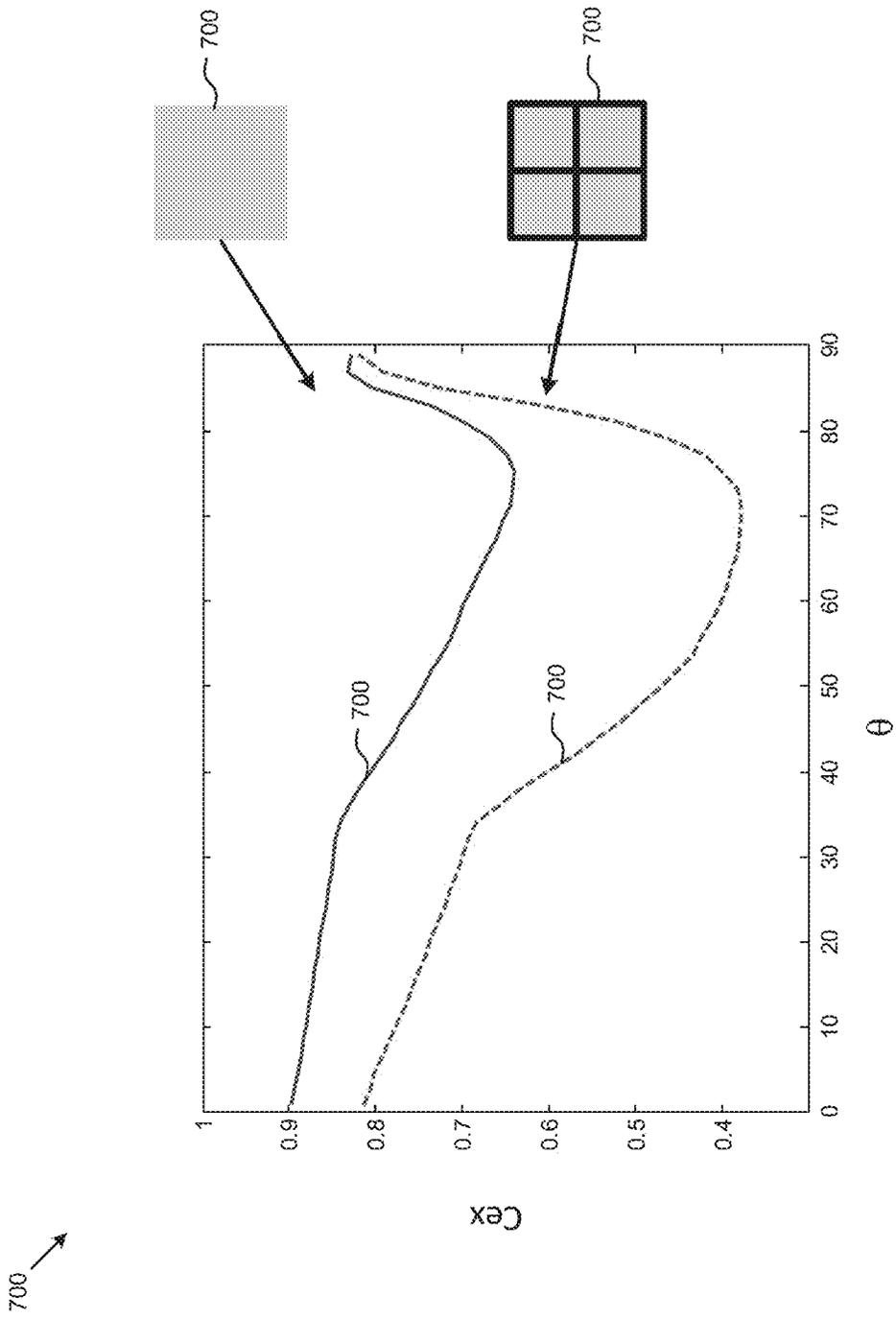


FIG. 7

800 →

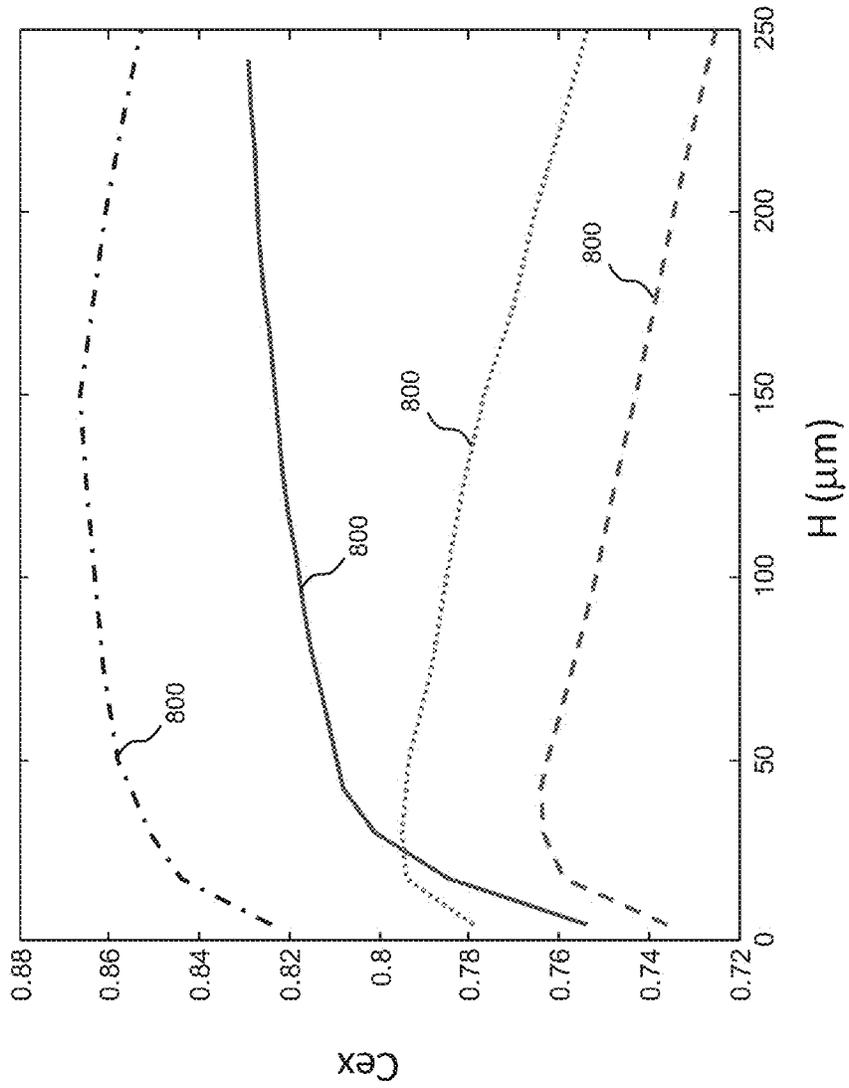


FIG. 8

900 ↗

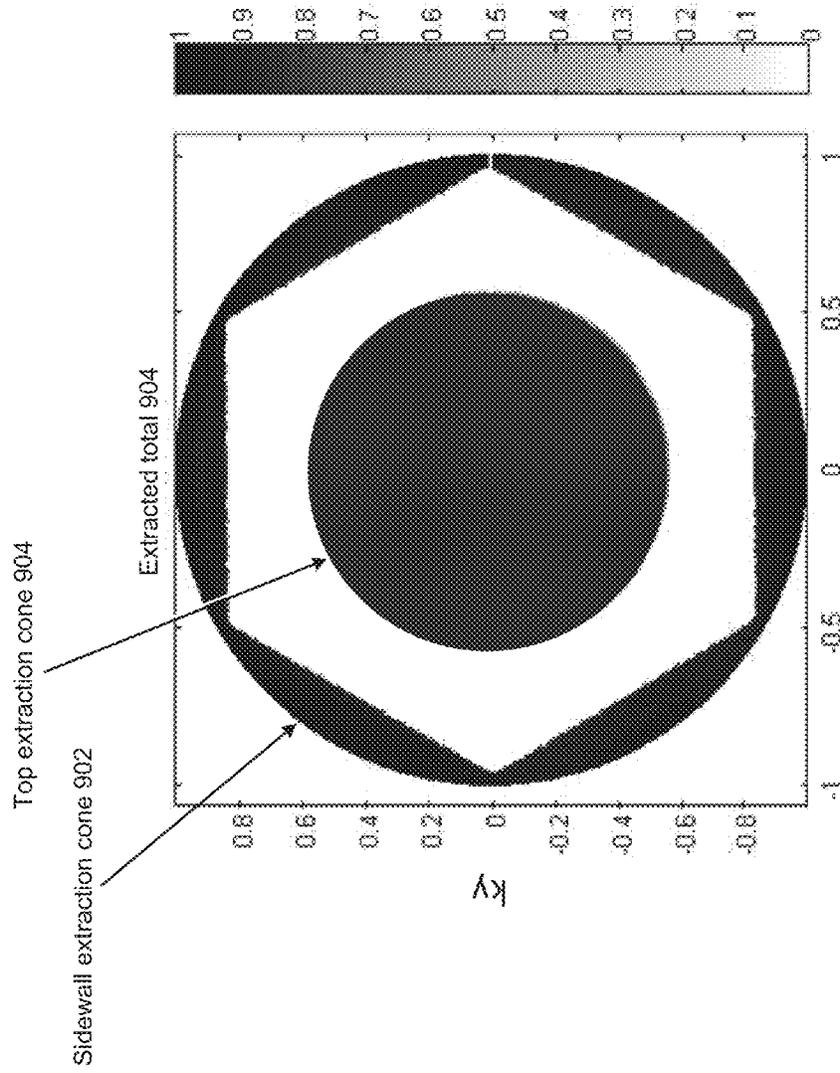


FIG. 9

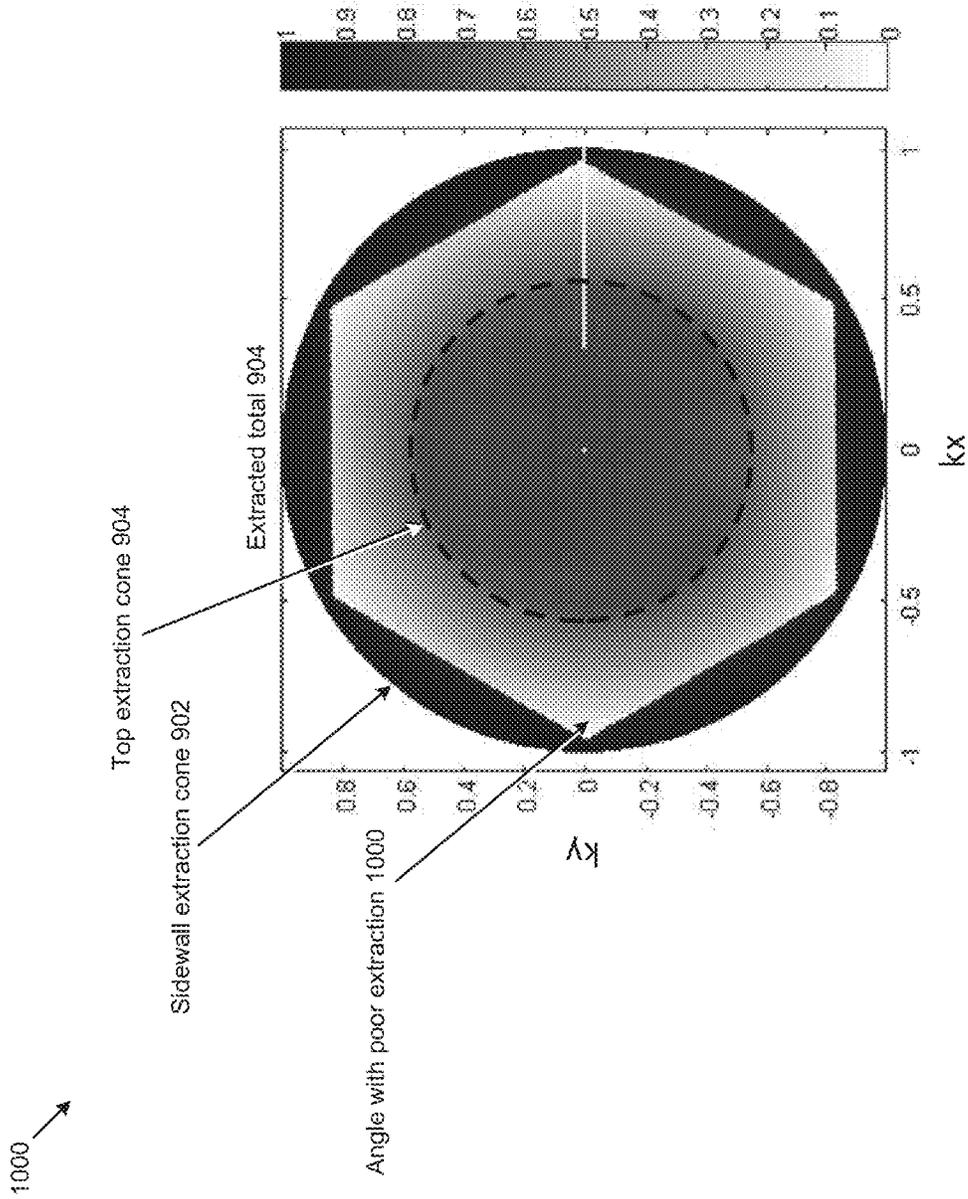


FIG. 10

1100

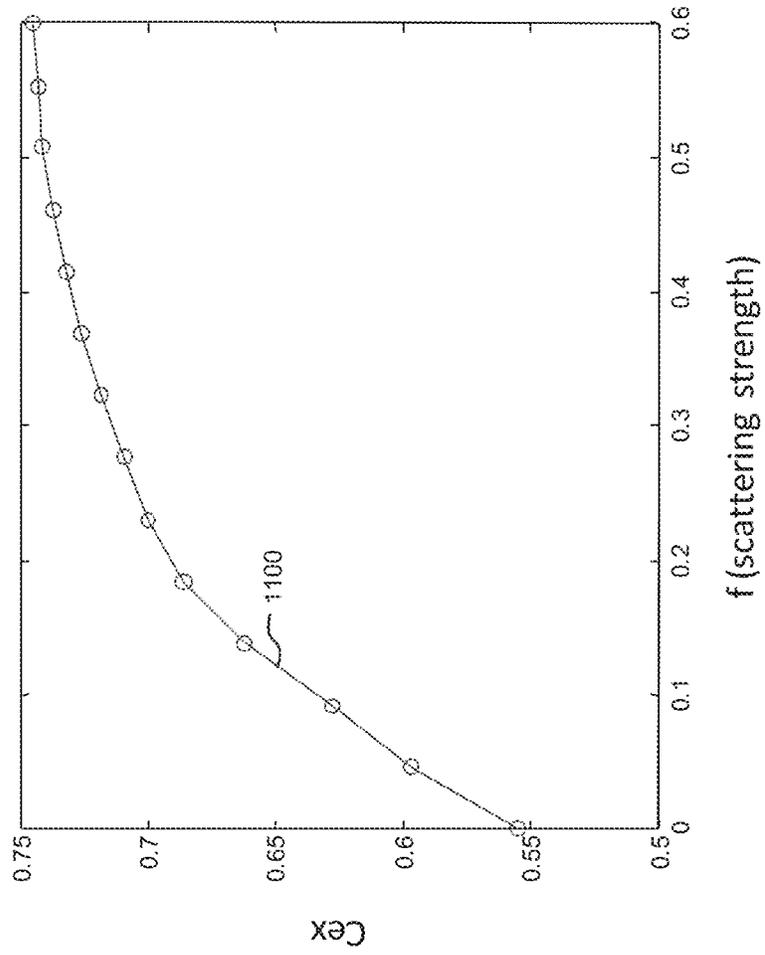


FIG. 11

1200 ↗

Top Surfaces 1202

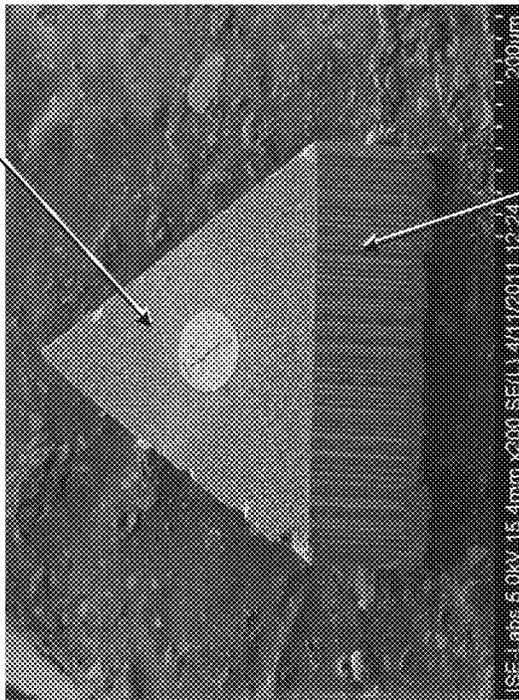
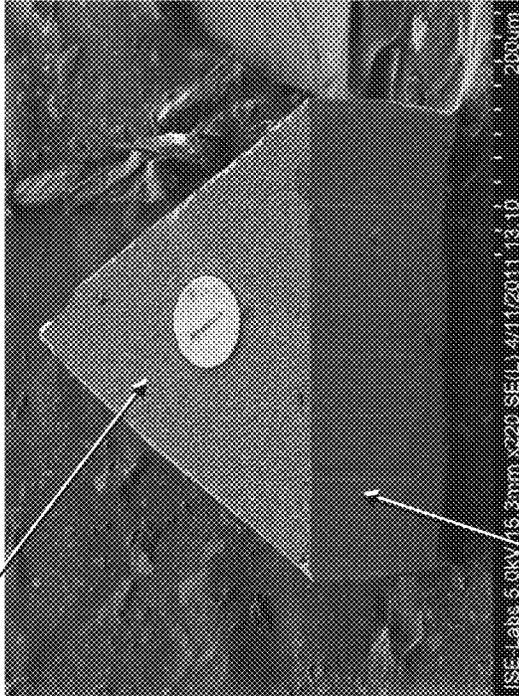


FIG. 12

1300 ↗

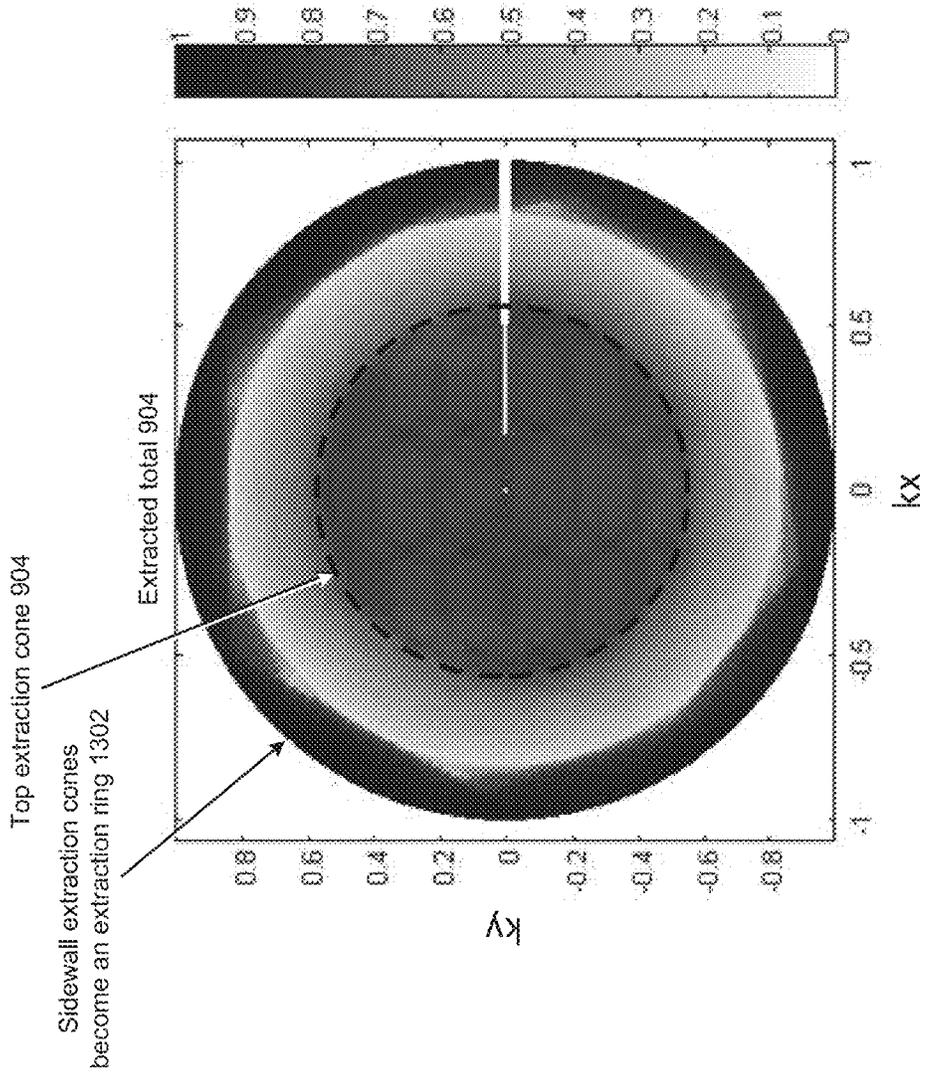


FIG. 13

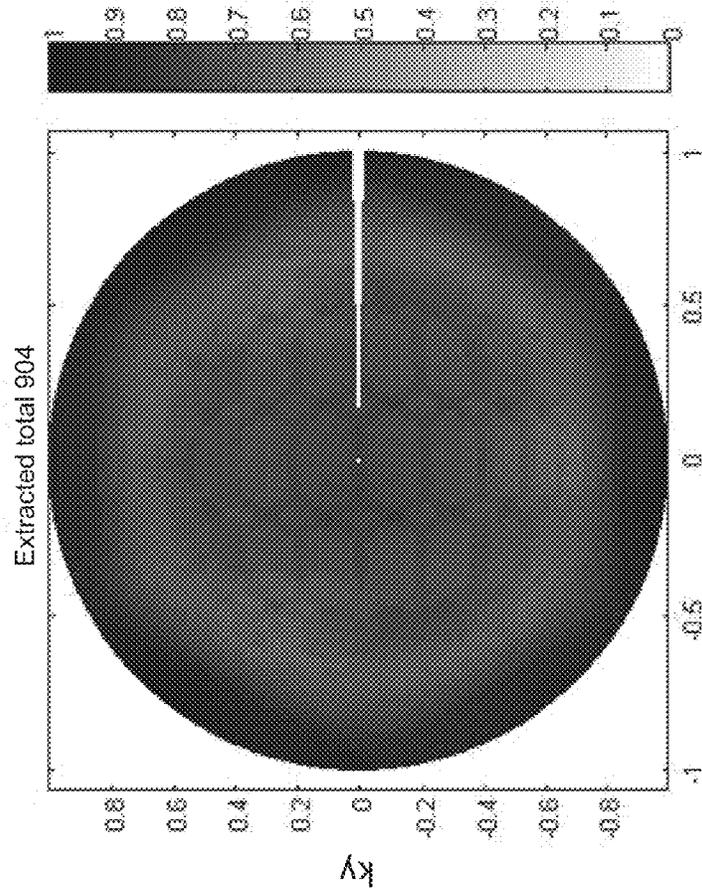


FIG. 14

1400 →

1500 ↗

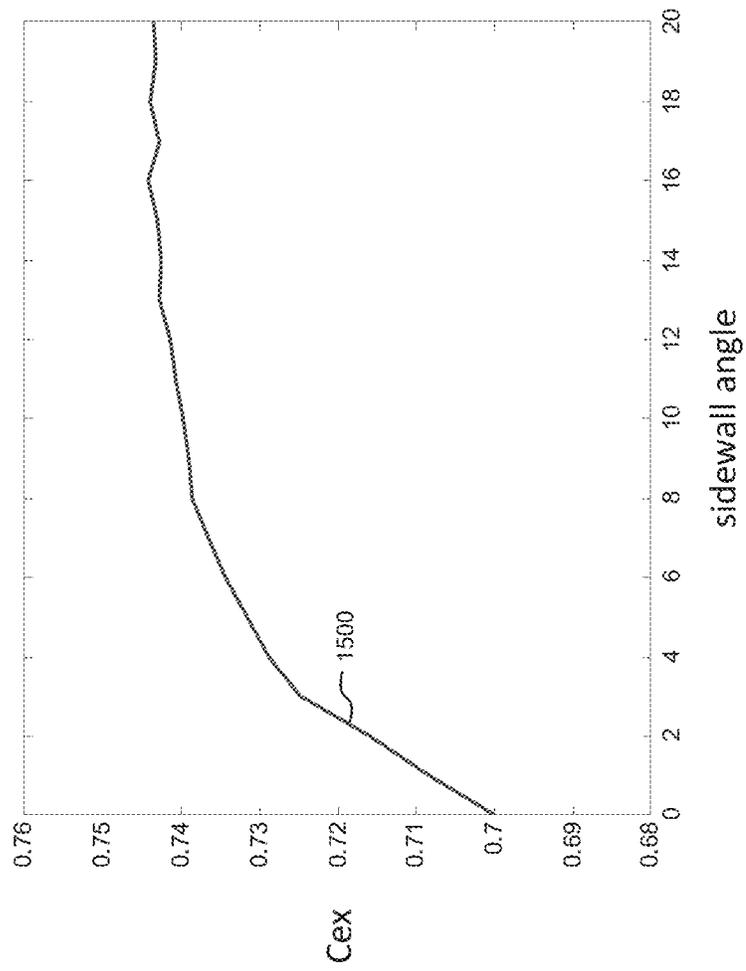


FIG. 15

1600 ↗

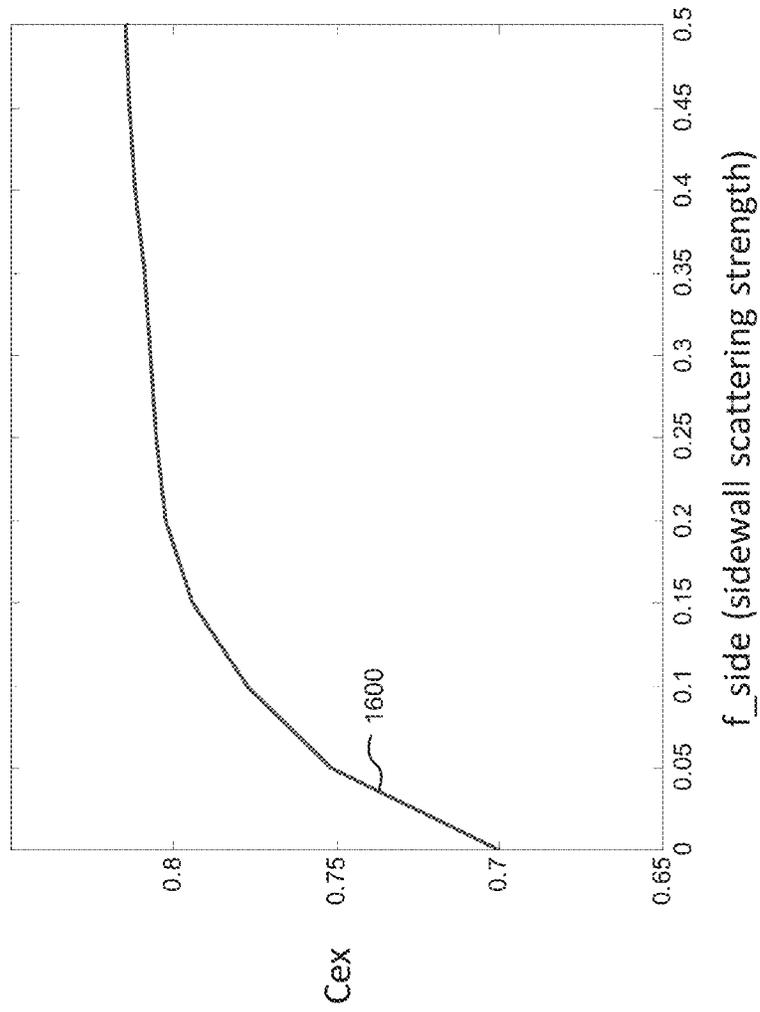


FIG. 16

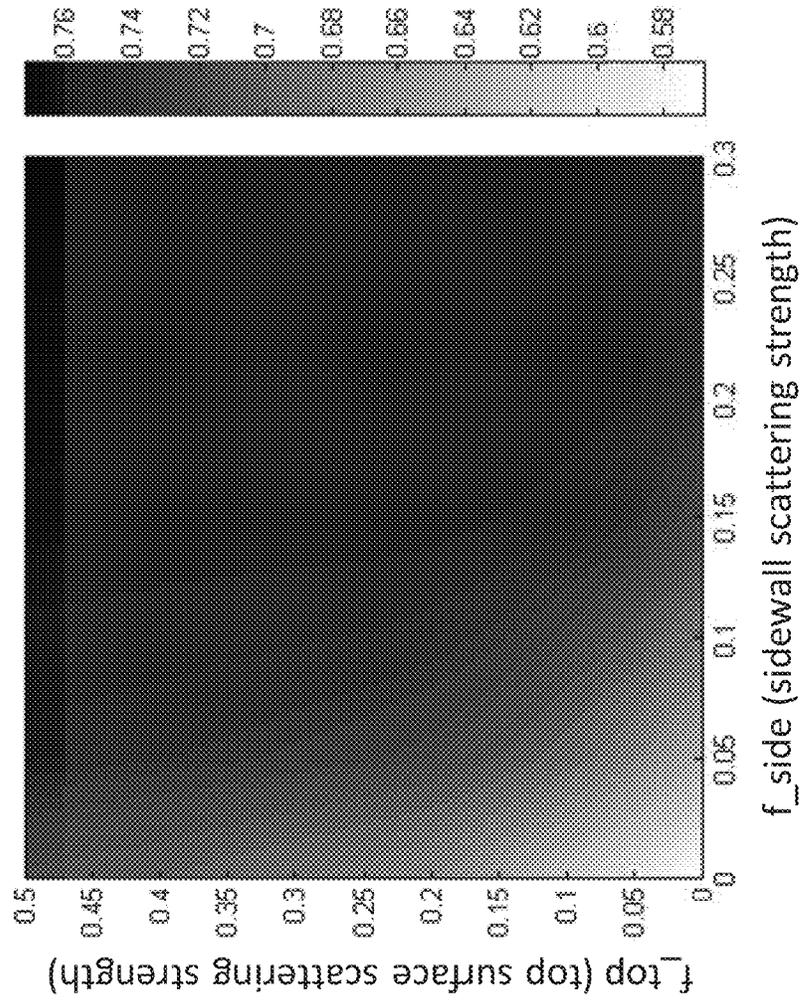


FIG. 17

1700 

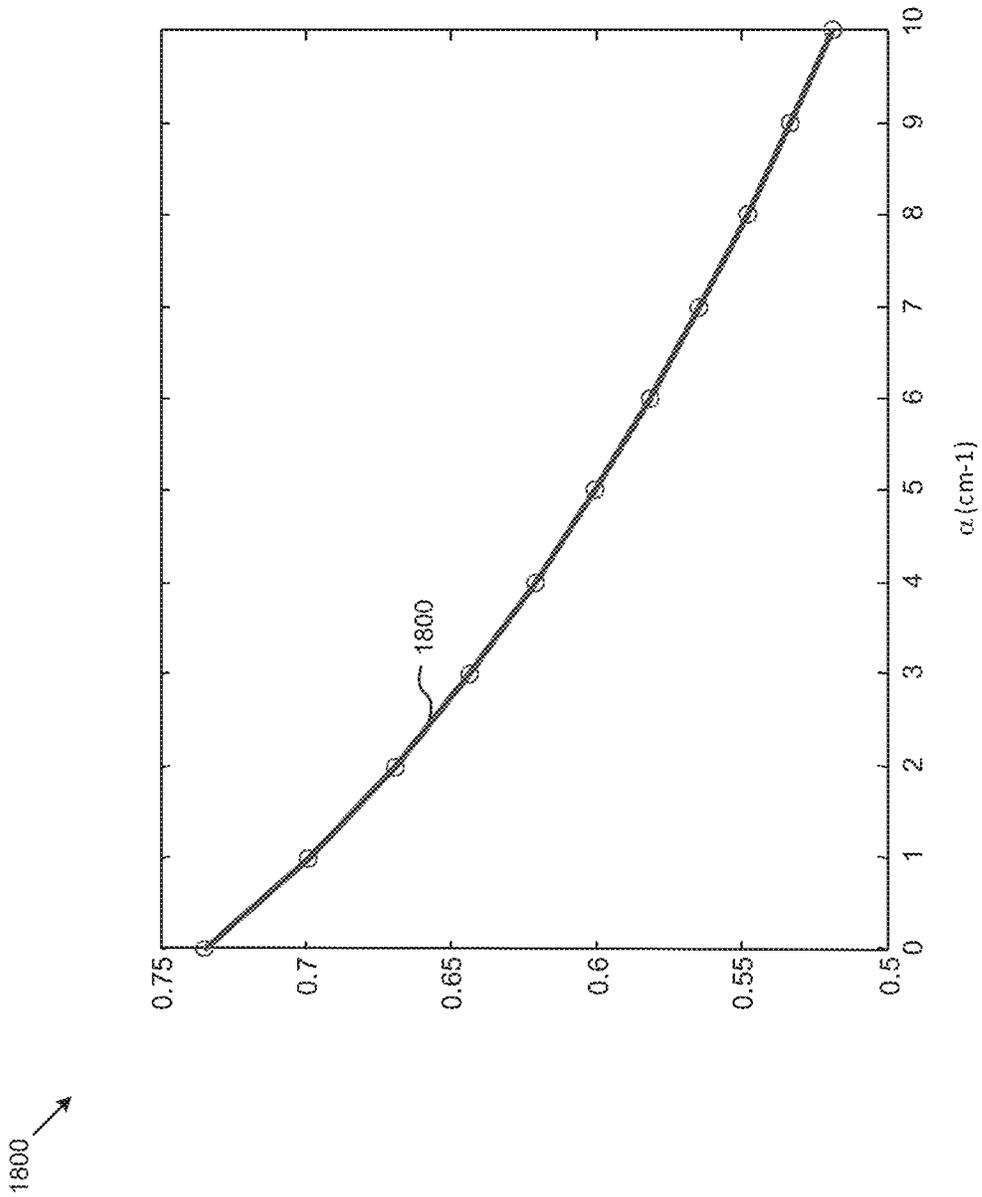


FIG. 18

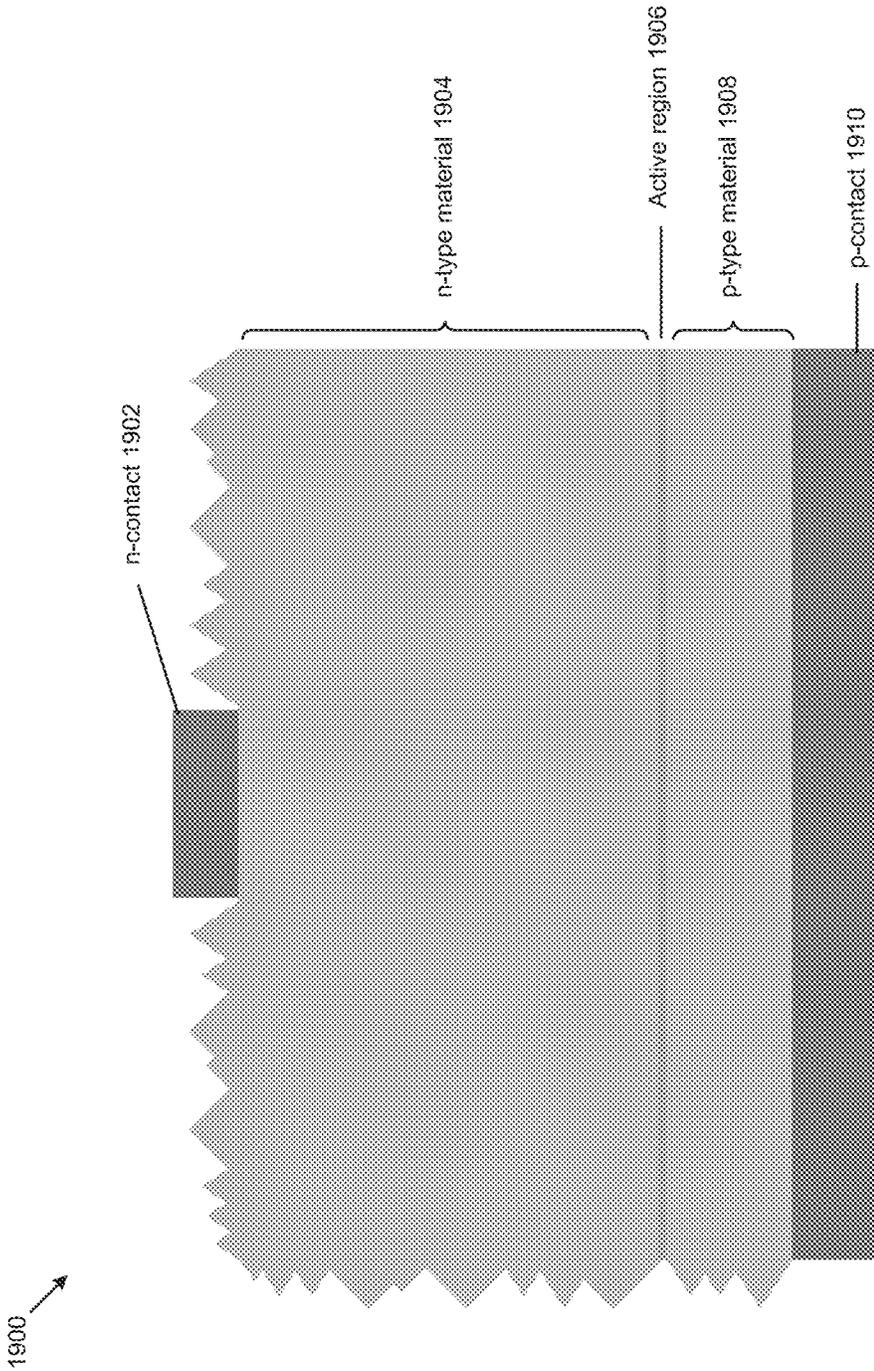


FIG. 19

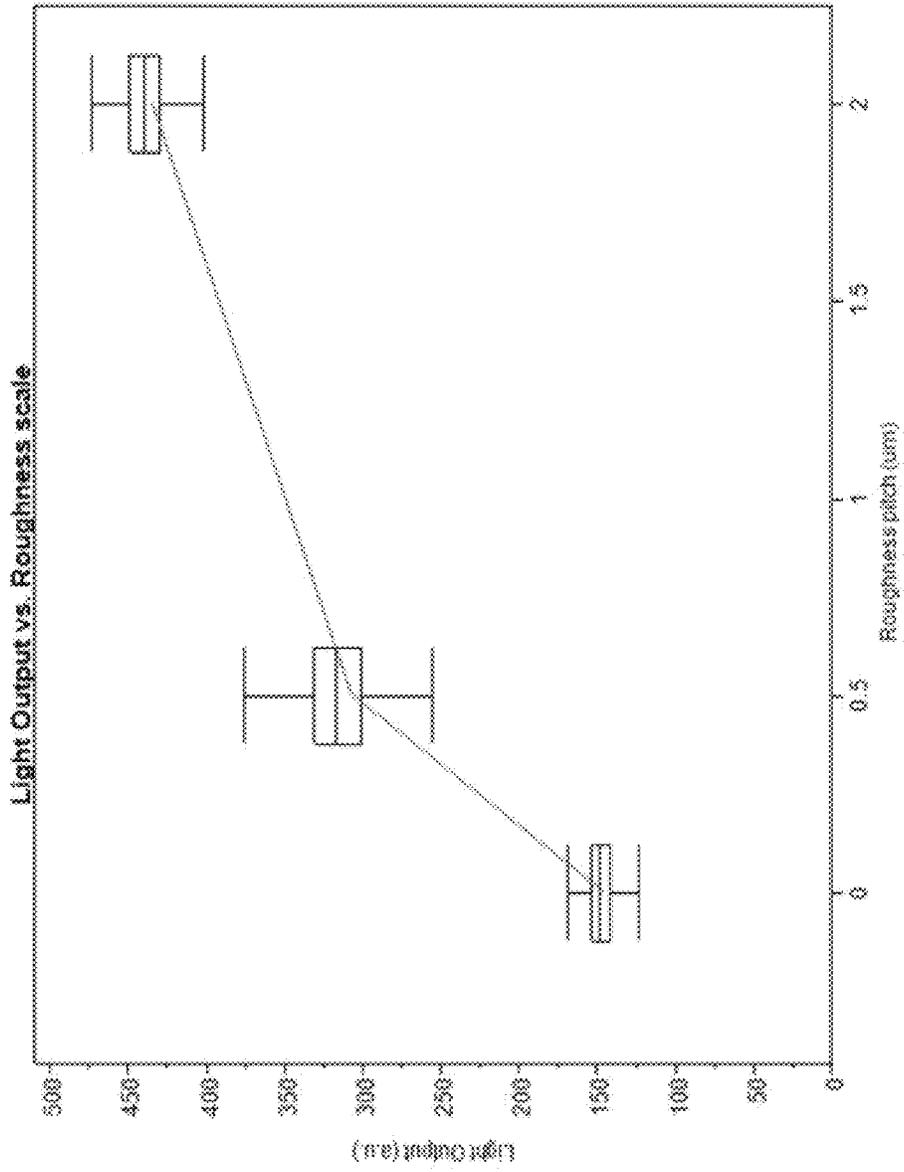


FIG. 20

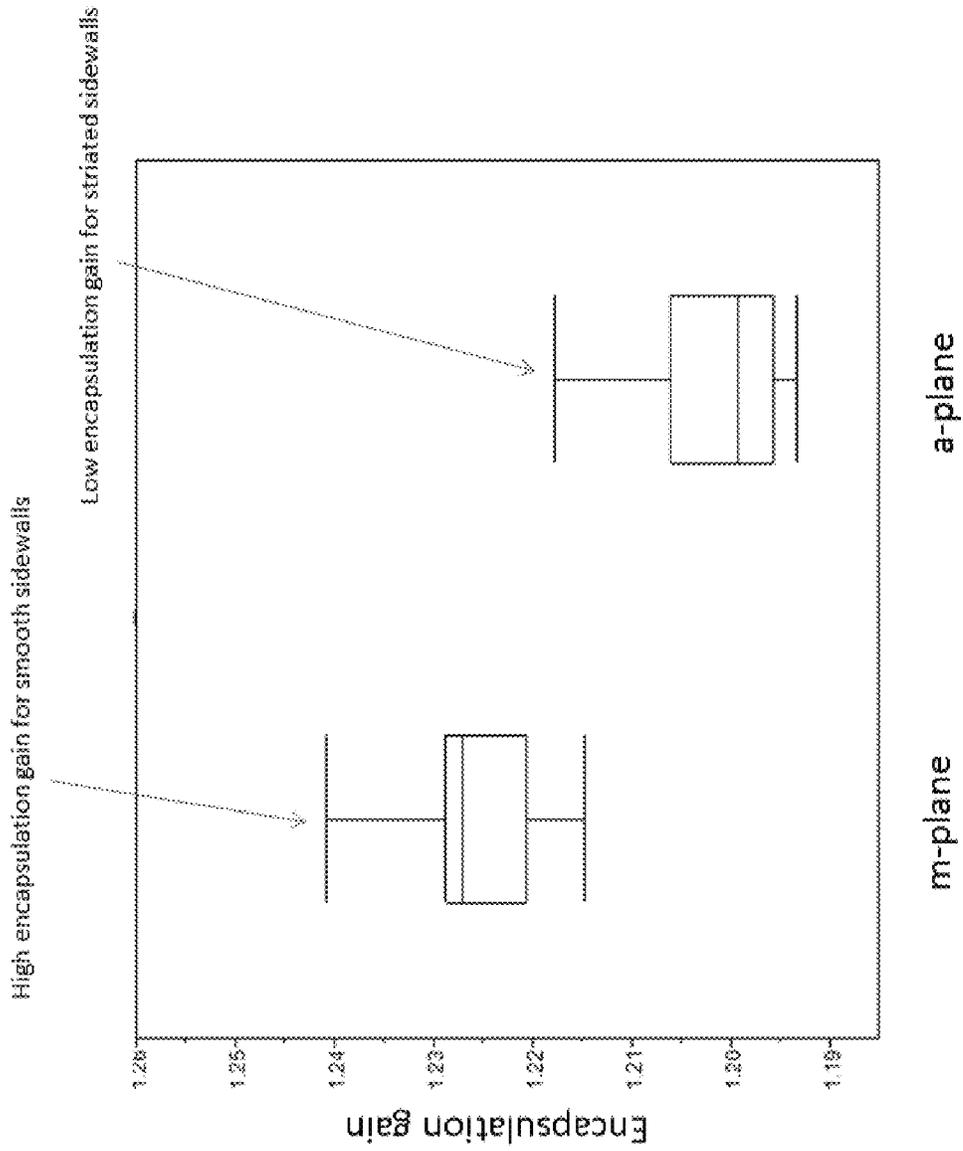
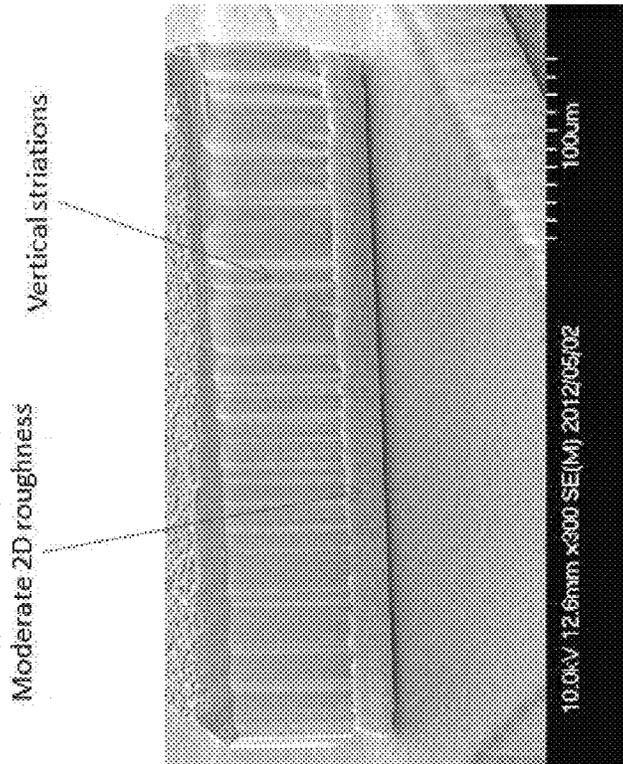
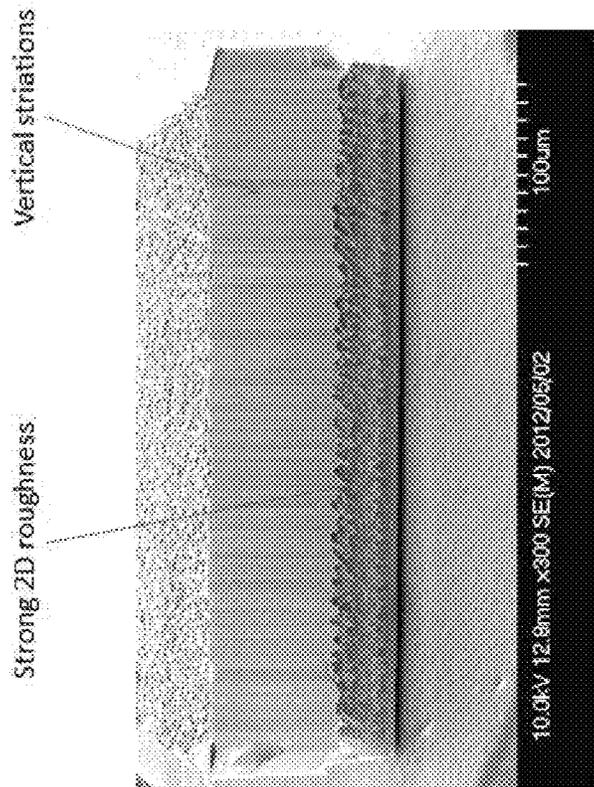


Fig 21



Method 2



Method 1

Fig 22

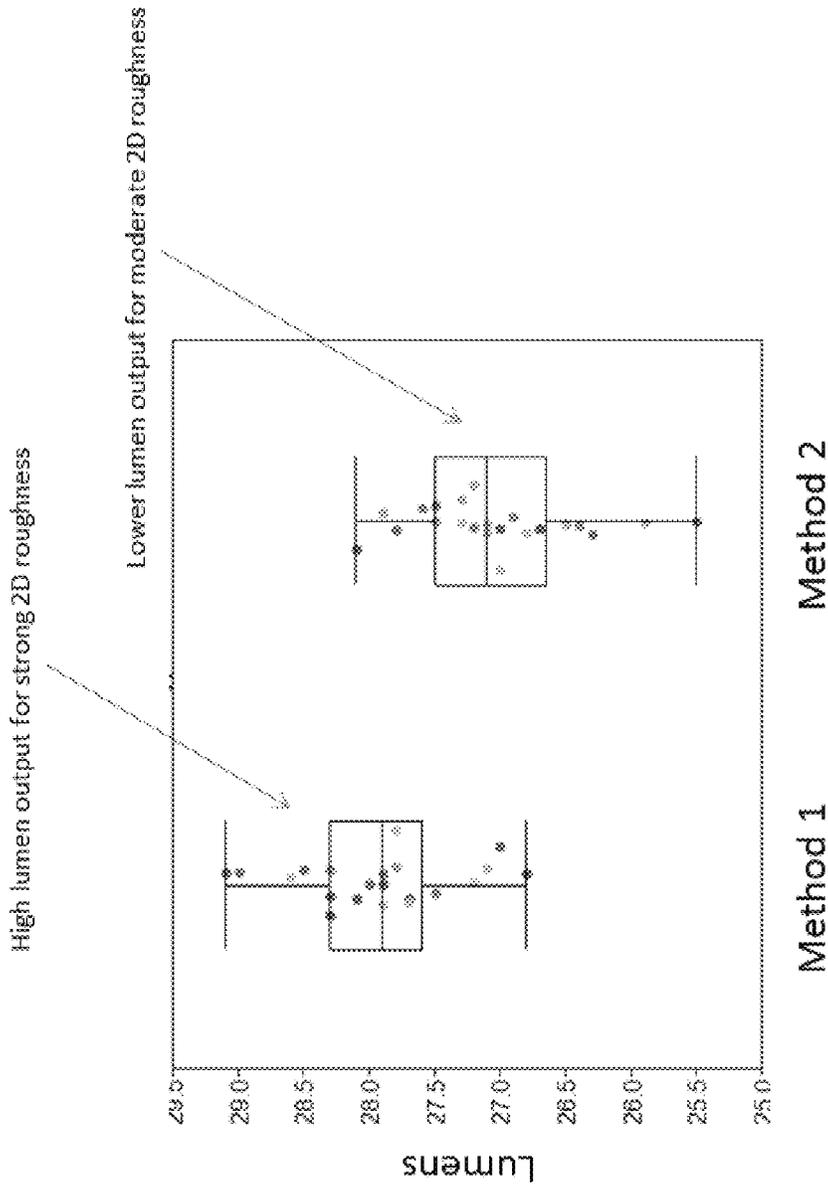


Fig 23

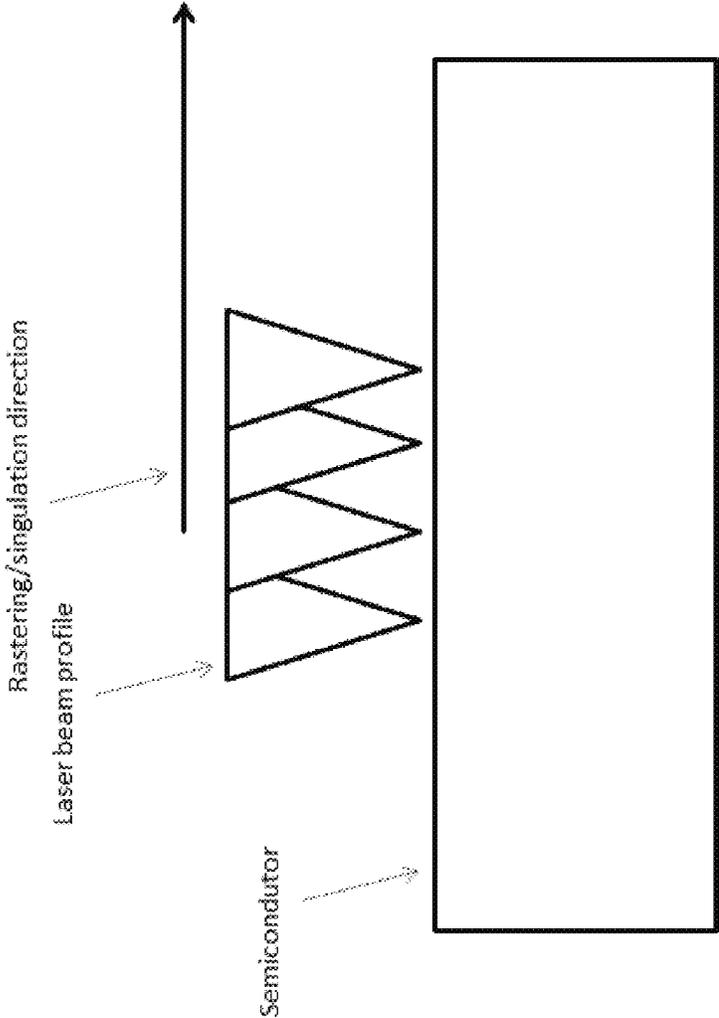


Fig 24

METHODS AND DEVICES FOR LIGHT EXTRACTION FROM A GROUP III-NITRIDE VOLUMETRIC LED USING SURFACE AND SIDEWALL ROUGHENING

This application is a continuation application of U.S. application Ser. No. 13/781,633 filed on Feb. 28, 2013, issued as U.S. Pat. No. 9,000,466, which is a continuation-in-part of U.S. application Ser. No. 12/861,765, filed on Aug. 23, 2010, and which claims the benefit under 35 U.S.C. §119(e) of U.S. Provisional Patent Application No. 61/605,026 filed on Feb. 29, 2012, each of which is incorporated by reference in its entirety.

FIELD

The disclosure relates to the field of LED light chips, and more particularly to techniques for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening.

BACKGROUND

The present disclosures are directed to an improved approach for achieving high-performance light extraction from a Group III-nitride volumetric LED chips. More particularly, disclosed herein are techniques for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening.

In making LED chips, improving the performance of light extraction from the material is an important design consideration. In some situations patterning or roughening of certain surfaces can improve light extraction. And, in some situations the materials used in making LEDs (e.g., GaN, Sapphire, SiC) are scribed, sawed, cleaved and otherwise manipulated during process such that those processes result in patterning or roughening of the surfaces of the LED device and/or surrounding structures. However, when Group III-nitride materials (e.g., gallium nitride) is used, traditional cleaving or other manipulations do not necessarily result in patterning or roughening of the surfaces of the LED device and/or surrounding structures, and other techniques are called for in order to achieve high-performance light extraction.

Moreover, the manufacture of Group III-nitride volumetric LED chips might involve cleaving along certain selected planes (e.g., c-plane, m-plane), and certain specific processing techniques (e.g., laser scribing) might be used with the Group III-nitride material, thus further demanding advances in the techniques to produce Group III-nitride volumetric LED chips that exhibit high-performance light extraction from surface and sidewall roughening.

Therefore, there is a need for an improved approach for achieving high-performance light extraction from Group III-nitride volumetric LED chips. In the approach to achieve high-performance light extraction from surface and sidewall roughening when using Group III-nitride materials, many discoveries have been made, which discoveries and embodiments thereto are disclosed in detail below.

SUMMARY

Embodiments of the present disclosures are directed to improved approaches for achieving high-performance light extraction from a Group III-nitride volumetric LED chips. More particularly, disclosed herein are techniques for achiev-

ing high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening.

The present disclosure provides improved techniques to address the aforementioned issues with legacy approaches. More specifically, the present disclosure provides a detailed description of surface and sidewall roughening techniques used to achieve high-performance light extraction from Group III-nitride volumetric LED chips.

The methods refer generally to GaN-based light emitting diodes grown on sapphire, SiC or similar heteroepitaxial substrate. In a specific embodiment, the present techniques provide a device configuration with a high extraction geometry, and fabrication method thereof, for a GaN-based light emitting diode overlying a bulk-GaN containing substrate.

Volumetric chips (e.g., chips where the vertical-to-horizontal aspect ratio of the chip is greater than 5%, and can be on the order of 100% or larger) are advantageous, because they benefit from additional extraction from the sidewalls (e.g., lateral surfaces) of the chip. This helps to extract glancing-angle light. In order to further increase light extraction, one can modify the sidewall facets in order to break these quasi-guided trajectories. This can be done by texturing of the sidewall facets. One way to texture the sidewalls is to produce 1-dimensional roughness, such as vertical striations.

Yet, improvements in extraction efficiency can be achieved by implementing 1-dimensional and 2-dimensional sidewall roughening. In some embodiments, the extraction efficiency for a chip with only top roughness is 70%. With combinations of 1D and 2D sidewall roughness, light extraction is boosted to ~82%.

Further details of aspects, objects, and advantages of the disclosure are described below in the detailed description, drawings, and claims. Both the foregoing general description of the background and the following detailed description are exemplary and explanatory, and are not intended to be limiting as to the scope of the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a chart characterizing backscattering behavior as a function of polar angle of incidence for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 2 is a simplified diagram of a model exhibiting backscattering behavior for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 3 is a chart characterizing backscattering behavior as a function of polar angle of incidence with various roughening patterns for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 4 is a chart characterizing light extraction as a function of top surface roughness for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 5 is a chart characterizing light extraction as a function of polar emission angle for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 6 is a chart characterizing light extraction as a function of n-grid width for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 7 is a chart characterizing light extraction as a function of polar emission angle, and showing n-grid width examples for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 8 is a chart characterizing light extraction as a function of chip height and showing examples varying lateral dimensions for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 9 is a chart characterizing extraction as a function of varied polar and azimuthal angles for a smooth volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip, according to some embodiments.

FIG. 10 is a chart showing light extraction as a function of varied polar and azimuthal angles for a surface-roughened volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 11 is a chart showing light extraction as a function of varied polar and azimuthal angles for top surface-roughness for a volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface roughening, according to some embodiments.

FIG. 12 shows images of LED chips formed by various cleaving along different crystallographic planes, according to some embodiments.

FIG. 13 is a chart showing light extraction as a function of varied polar and azimuthal angles for 1D roughened sidewall surfaces for a volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 14 is a chart showing light extraction as a function of varied polar and azimuthal angles for 2D roughened sidewall surfaces for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 15 is a chart showing light extraction for 1D roughened sidewall surfaces as a function of sidewall angle for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 16 is a chart showing light extraction for 2D roughened sidewall surfaces as a function of sidewall angle for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 17 is a chart showing light extraction under varied sidewall and top roughness for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 18 is a chart showing light extraction under varied substrate absorption for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 19 is a simplified schematic diagram of a light emitting diode device having a top surface region with a textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm; and a lateral surface region having a

textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening, according to some embodiments.

FIG. 20 shows light extraction as a function of roughness, according to some embodiments.

FIG. 21 shows the encapsulation gain performance of LED chips formed by various cleaving along different crystallographic planes, according to some embodiments.

FIG. 22 depicts SEM images of LED chips formed by various laser scribing processes, according to some embodiments.

FIG. 23 shows the lumen output performance of LED chips formed by various laser scribing processes, according to some embodiments.

FIG. 24 shows the beam profile of a multiple-beam laser ablation tool used in the singulation process of LEDs.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Various embodiments will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments are shown. Various aspects may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

Embodiments of the present disclosures are directed to improved approaches for achieving high-performance light extraction from a Group III-nitride volumetric LED chips. More particularly, disclosed herein are techniques for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening.

In making LED chips, improving the performance of light extraction from the material is an important design consideration. In some situations patterning or roughening of certain surfaces can improve light extraction. And, in some situations the materials used in making LEDs (e.g., GaN, Sapphire, SiC) are scribed, sawed, cleaved and otherwise manipulated during process such that those processes result in patterning or roughening of the surfaces of the LED device and/or surrounding structures. However, when Group III-nitride materials (e.g., gallium nitride) is used, traditional cleaving or other manipulations do not necessarily result in patterning or roughening of the surfaces of the LED device and/or surrounding structures, and other techniques are called for in order to achieve high-performance light extraction.

Moreover, the manufacture of Group III-nitride volumetric LED chips might involve cleaving along certain selected planes (e.g., c-plane, m-plane), and certain processing techniques (e.g., laser scribing) might be used with the Group III-nitride material, thus further demanding advances in the techniques to produce Group III-nitride volumetric LED chips that exhibit high-performance light extraction from surface and sidewall roughening.

Therefore, there is a need for an improved approach for achieving high-performance light extraction from Group III-nitride volumetric LED chips. In the approach to achieve high-performance light extraction from surface and sidewall roughening when using Group III-nitride materials, many discoveries have been made, which discoveries and embodiments thereto are disclosed in detail below.

Embodiments of the present disclosure provide improved techniques to address the aforementioned issues with legacy approaches. More specifically, the present disclosure provides a detailed description of surface and sidewall roughening techniques used to achieve high-performance light extraction from Group III-nitride volumetric LED chips.

The methods refer generally to GaN-based light emitting diodes grown on sapphire, SiC or similar heteroepitaxial substrate. In an embodiment, the present techniques provide a device configuration with a high extraction geometry, and fabrication method thereof, for a GaN-based light emitting diode overlying a bulk-GaN containing substrate.

Volumetric chips (e.g., chips where the vertical-to-horizontal aspect ratio of the chip is greater than 5%, and can be on the order of 100% or larger) are advantageous, because they benefit from additional extraction from the sidewalls (e.g., lateral surfaces) of the chip. This helps to extract glancing-angle light. In order to further increase light extraction, one can modify the sidewall facets in order to break these quasi-guided trajectories. This can be done by texturing of the sidewall facets. One way to texture the sidewalls is to produce 1-dimensional roughness, such as vertical striations.

Yet, improvements in extraction efficiency can be achieved by implementing 1-dimensional and 2-dimensional sidewall roughening. In some embodiments, the extraction efficiency for a chip with only top roughness is 70%. With combinations of 1D and 2D sidewall roughness, light extraction is boosted to ~82%.

As used herein, the term GaN substrate is associated with Group III-nitride based materials including GaN, InGa_N, AlGa_N, or other Group III containing alloys or compositions that are used as starting materials. Such starting materials include polar GaN substrates (i.e., substrate where the largest area surface is nominally an (h k l) plane where h=k=0, and l is non-zero), non-polar GaN substrates (i.e., substrate material where the largest area surface is oriented at an angle ranging from about 80-100 degrees from the polar orientation described above towards an (h k l) plane where l=0, and at least one of h and k is non-zero) or semi-polar GaN substrates (i.e., substrate material where the largest area surface is oriented at an angle ranging from about +0.1 to 80 degrees or 110-179.9 degrees from the polar orientation described above towards an (h k l) plane where l=0, and at least one of h and k is non-zero). Of course, there can be other variations, modifications, and alternatives.

The high-refractive index of Group III-nitride based semiconductor devices results in a large fraction of emitted light being totally-internally reflected at the semiconductor/air or semiconductor/encapsulant interface on the first pass. The embodiments contained herein provides methods for enhancing the fraction of emitted light from a light emitting diode device which escapes the semiconductor/air or semiconductor/encapsulant interface on the first pass, and thereby improving the overall external quantum efficiency of the light emitting diode device. This is achieved through texturing or roughening of the sidewalls or side-surfaces of a light emitting diode device chip by applying the methods described in the embodiments below, so as to enhance the extraction of light from these sidewalls or side-surfaces.

For high-power chips, a wafer-bonded geometry is usually used for thermal management. In this case the p-side of the chip is covered by a reflective contact and light is mostly extracted through the top side. To increase light extraction, this top surface is typically roughened in order to randomize light trajectories and avoid guiding of light. To understand how surface roughness improves light extraction in an LED, we model its scattering properties. In the following, we assume

roughening features with an average lateral distance on the order of ~1 μm, as is typically obtained by processes such as chemical etching or photo-electro-chemical etching and present in commercial Group III-nitride LEDs. The parameter which drives the scattering strength in the calculations shown below is the so-called filling fraction f , e.g. the area coverage of the scattering features. A small filling fraction corresponds to scattering features with narrow lateral dimensions separated by flat regions, while $f > 0.5$ is representative of GaN roughnesses in some commercial LEDs. The scattering properties of such a surface are illustrated on FIG. 1, which represents the one-bounce backscattering S_b (e.g., the amount of light which is sent back in the semiconductor) for a typical embodiment of a rough surface. A low backscattering corresponds to a large forward-scattering, and hence a large light extraction.

An important parameter in describing a rough surface is the characteristic size of the features forming the roughness. In typical embodiments, this characteristic size is related to the wavelength of light λ and the index of the LED material n . For instance, in some embodiments, the characteristic size is larger than 0.1 time λ/n and smaller than 30 times λ/n . The roughness of the surface can further be described in terms of the shape of features that form the roughened surface. For instance, the roughness can be one-dimensional (e.g. linear striations) or two-dimensional (e.g., surface variations in both in-plane directions). Further, two-dimensional roughness can be composed of a variety of shapes such as pyramidal features, truncated pyramidal features, cylindrical features, square features, spherical features, elliptical features, or a combination of these shapes.

FIG. 1 is a chart characterizing backscattering behavior as a function of polar angle of incidence for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing backscattering behavior as a function of polar angle of incidence may be implemented in the context of the architecture and functionality of the embodiments described herein. Also, the method for characterizing backscattering behavior as a function of polar angle of incidence or any characteristic therein may be carried out in any desired environment. FIG. 1 shows that S_b becomes close to unity for angles larger than 70°. This indicates that extraction to the outside of the chip is not efficient, and that light will need many bounces to be extracted. FIG. 1 illustrates backscattering of a typical patterned surface versus polar angle of incidence θ (averaged over the azimuthal angle ϕ). Here the surface is a GaN/epoxy interface made of cylindrical rods (filling fraction $f=0.3$), height h averaged from 0.8 to 1.2, pitch averaged from 0.8 to 1.2). All distances in units of the free wavelength λ .

From this, we conclude that contrary to intuition, typical 'random' surfaces in LEDs do not necessarily fully randomize light trajectory—most notably, light propagating near glancing angles is poorly extracted/diffused, and mostly undergoes specular reflection. FIG. 2 schematically represents this behavior.

FIG. 2 is a diagram of model exhibiting backscattering behavior for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model exhibiting backscattering behavior may be implemented in the context of the architecture and functionality of the embodiments described herein. As shown, the details of the roughness do not affect these results for features of a given size. FIG. 2 shows the schematic behavior of a typical roughened surface. Light propagating close to normal incidence

(thin lines) is efficiently extracted. However, for light propagating near glancing angle (thick lines), only a small fraction of the light is extracted (thick line) while a large fraction is backscattered.

FIG. 3 is a chart characterizing backscattering behavior as a function of polar angle of incidence with various roughening patterns for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing backscattering behavior as a function of polar angle of incidence with various roughening patterns may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 3 illustrates structural features by comparing the scattering behavior of periodic structures having cylindrical and pyramidal features. In this calculation, the rough features have similar sizes, and show similar scattering behavior. This result can be extended to disordered structures by use of a supercell model which considers a periodic structure with a large period whose unit cell is composed of several scattering elements of varying shape and size, and thus approximates the description of a disordered rough surface. Again, use such of a supercell model shows a very similar scattering behavior to that shown in FIG. 3. These scattering properties can be integrated to a ray-tracing light extraction model in order to describe realistic LED chips and understand how the scattering properties impact light extraction. Below are described various applications of such a model to selected geometries of interest. FIG. 3 shows backscattering of various rough surfaces versus polar angle of incidence q : (solid line): cylindrical rods (height averaged from 0.8 to 1.2). Dashed line: pyramids (height 1). Dotted lines: pyramids (height 0.6). All distances in units of the free wavelength λ . All structures have a filling fraction $f=0.3$.

Thin-Film Chips

Thin-film chips (where the ratio of vertical-to-horizontal dimensions is less than 5%, and often less than 1%) are strongly affected by the scattering behavior of the scattering surface. This is illustrated in FIG. 4 which shows the extraction efficiency C_{ex} of a 1 mm \times 1 mm \times 5 μ m chip (typical dimensions for commercial power chips) with top surface roughness, as a function of the reflectivity R of the p-mirror. In this simple model, the p-mirror is the only source of loss. A large value of R is necessary to obtain high $C_{ex}>80\%$ due to the difficulty to extract glancing-angle light. Additional models (e.g., that model additional characteristics beyond the model of FIG. 4) show similar results.

FIG. 4 is a chart characterizing light extraction as a function of top surface roughness for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing light extraction as a function of top surface roughness may be implemented in the context of the architecture and functionality of the embodiments described herein. FIG. 4 shows a square thin-film chip (1 mm \times 1 mm \times 5 μ m) with a top surface roughness and varying p-mirror reflectivity.

In this simple model, the p-mirror is the only source of loss. A large value of R is necessary to obtain high $C_{ex}>80\%$ due to the difficulty to extract glancing-angle light. This is illustrated in FIG. 5.

FIG. 5 is a chart characterizing light extraction as a function of polar emission angle for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing light extraction as a function of

polar emission angle may be implemented in the context of the architecture and functionality of the embodiments described herein.

As shown, FIG. 5 details the extraction efficiency $C_{ex}(\theta)$ versus the polar angle of emission θ (averaged over the azimuthal angle ϕ , and for a p-mirror reflectivity $R=90\%$), and shows a collapse of C_{ex} at large θ . This situation is made even worse if we take into account additional absorbing features (such as n-electrodes) that are present in chips. FIG. 6 illustrates this situation. FIG. 5 shows a square chip (1 mm \times 1 mm \times 5 μ m) with a top surface roughness and $R=90\%$ p-mirror reflectively and details of extraction efficiency as a function of polar emission angle θ (averaged over the azimuthal angle of emission Φ). Angle around 50° to 85° are poorly extracted.

FIG. 6 is a chart characterizing light extraction as a function of n-grid width for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing light extraction as a function of n-grid width may be implemented in the context of the architecture and functionality of the embodiments described herein. Also, the method for characterizing light extraction as a function of n-grid width or any characteristic therein may be carried out in any desired environment. FIG. 6 shows a square chip (1 mm \times 1 mm) with a top surface roughness and $R=90\%$ p-mirror reflectively, varying n-grid width.

The chip of FIG. 6 depicts a chip of similar dimensions but with a square n-grid of pitch $a=250 \mu$ m, and of low reflectivity ($R=50\%$) and varying grid width w . As w increases, C_{ex} is strongly impacted—this is because glancing-angle light travels large lateral distances and has a high probability of reaching the lossy n-grid. Again, this is seen in detail in FIG. 7.

FIG. 7 is a chart characterizing light extraction as a function of polar emission angle, and showing n-grid width examples for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing light extraction as a function of polar emission angle, and showing n-grid width examples may be implemented in the context of the architecture and functionality of the embodiments described herein. Also, the techniques for characterizing light extraction as a function of polar emission angle, and showing n-grid width examples or any characteristic therein may be carried out in any desired environment. FIG. 7 shows a square chip (1 mm \times 1 mm) with top surface roughness and $R=90\%$ p-mirror reflective and details of extraction efficiency as a function of polar emission angle θ . Full lines refer to no n-grid and dashed lines to 15 μ m-wide n-grid.

FIG. 7 shows the same angle-dependent light extraction $C_{ex}(\theta)$ as is shown in FIG. 5 (for $w=15 \mu$ m), and where the suppression of C_{ex} at large θ is even more pronounced. Surface-Roughened Volumetric Chips

Volumetric chips (e.g., chips where the vertical-to-horizontal aspect ratio of the chip is greater than 5%, and can be on the order of 100% or larger) are advantageous, because they benefit from additional extraction from the sidewalls (e.g., lateral surfaces) of the chip. This helps to extract glancing-angle light.

FIG. 8 is a chart characterizing light extraction as a function of chip height and showing examples of varying lateral dimensions for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model characterizing light extraction as a function of chip height and showing examples varying lateral dimensions may be imple-

mented in the context of the architecture and functionality of the embodiments described herein.

FIG. 8 shows how increasing the thickness of a chip increases its extraction efficiency. First we consider a 1×1 mm surface-roughened chip, with p-mirror reflectivity $R=90\%$. Increasing the thickness from 5 μm to 250 μm boosts the extraction from $\sim 75\%$ to $\sim 83\%$, because large-angle light can now be extracted by the sidewalls (e.g., lateral surfaces). However, substrate loss can be present and hinder the beneficial effect of volumetric chips. If we assume a GaN absorption coefficient $\alpha=1\text{ cm}^{-1}$, extraction is significantly impacted. This can be improved upon by reducing the lateral dimensions of the chip: with the same α , a 250×250 μm chip is about 4% more efficient than a 1 mm×1 mm chip. The beneficial impact of sidewalls for light extraction can further be improved by modifying the shape of the chip. For instance, using a chip with a triangular base and the same surface area enables more light trajectories to be extracted. From FIG. 8, the advantage of volumetric chips can be leveraged when the chip dimensions and shape are well chosen, considering the losses in the chip. FIG. 8 shows extraction efficiency vs. chip height, for chips with top surface roughness and $R=90\%$ p-mirror reflectivity: (solid line) 1 mm×1 mm square chip, no absorption in the GaN substrate; (dashed line) 1 mm×1 mm square chip, GaN absorption coefficient $a=1\text{ cm}^{-1}$; (dotted line) 250 μm ×250 μm square chip, GaN absorption coefficient $a=1\text{ cm}^{-1}$; (dash-dotted line) Triangular chip (lateral dimension 380 μm), GaN absorption coefficient $a=1\text{ cm}^{-1}$.

We note that while we have modeled particular chip designs in the above, and other models of chips, additional sources of loss can be considered, for example: substrate absorption, absorption of all the contacts (p- and n-electrodes and additional interlayers), active region absorption, etc. In some of the following descriptions, realistic values for such losses are modeled.

More insight can be gained into the light-extraction process of such volumetric chips by looking at the angle-resolved extraction diagram $C_{\text{ex}}(\theta, \phi)$ —here it is relevant to consider both angles. For simplicity, let us first consider a smooth (non-roughened) chip.

FIG. 9 is a chart showing extraction as a function of varied polar and azimuthal angles for a smooth volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model extraction as a function of varied polar and azimuthal angles for a smooth volumetric chip may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 9 models a smooth GaN volumetric chip (triangular base 380 μm , height 200 μm) emitting into a silicone of index $n=1.4$. Extraction is only possible into seven extraction cones (one for the top surface, and six for the three sidewalls—either directly or after one in-plane bounce), while all the rest of the light is guided and eventually lost. To improve the extraction of light, in volumetric chips, its top surface can be roughened, which roughening serves to break guided light trajectories. A similar surface roughening approach can also improve light extraction in thin-film chips. FIG. 9 shows details of extraction vs. polar (θ) and azimuthal (ϕ) angles, for a smooth volumetric chip with a triangular base (lateral dimension 380 μm , height 200 μm). The direction of emitted light is characterized by the in-plane reduced wavevectors k_x and k_y . High extraction is obtained into the top extraction cone and the six sidewall extraction cones. No extraction is possible outside of these cones.

FIG. 10 is a chart showing light extraction as a function of varied polar and azimuthal angles for a surface-roughened volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model light extraction as a function of varied polar and azimuthal angles for a surface-roughened volumetric chip may be implemented in the context of the architecture and functionality of the embodiments described herein.

As shown, FIG. 10 illustrates the modification of the angle-resolved extraction diagram when top surface roughness is implemented: Extraction is allowed for angles outside of the extraction cones. However, this is not perfectly efficient because light propagating at large angles is weakly randomized, as was the case for a thin-film chip. Large angles still display limited extraction. Such trajectories, which we refer to as “quasi-guided”, limit the extraction efficiency of a GaN volumetric chip with top surface roughness. FIG. 10 shows details of extraction vs. polar (θ) and azimuthal (ϕ) angles, for a volumetric chip with a triangular base (lateral dimension 380 μm , height 200 μm) with top surface roughness. Surface roughness enables extraction of some of the light outside of the extraction cones—however this effect is limited, especially at large angles.

FIG. 11 is a chart showing light extraction as a function of varied polar and azimuthal angles for top surface roughness for a volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model light extraction as a function of varied polar and azimuthal angles for top surface roughness for a volumetric chip may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 11 shows the total extraction efficiency of a volumetric surface roughness, as the scattering efficiency of the top roughness is varied. The extraction saturates for larger values of the scattering efficiency, because the top roughness never fully breaks quasi-guided trajectories. Here we used the roughness filling fraction as the scattering parameter. A similar result is obtained when increasing the size of the scattering features from $\sim 500\text{ nm}$ to $\sim 1.5\text{ }\mu\text{m}$. Therefore efficient scattering requires a filling fraction which is high enough (typically >0.5) and a feature size which is large enough (typically $\sim 1\text{ }\mu\text{m}$). However even using an optimized roughness, light extraction remains limited. FIG. 11 shows C_{ex} vs. top surface roughness for a GaN LED with a triangular base (lateral dimension 380 μm , height 200 μm) and with top surface roughness.

50 Sidewall-Roughened Volumetric Chips

In order to further increase light extraction, one can modify the sidewall facets in order to break these quasi-guided trajectories. This can be done by texturing of the sidewall facets. One way to texture the sidewalls is to produce 1-dimensional roughness, such as vertical striations. Such striations can naturally be obtained by using a die cleaving method along a proper crystal plane.

FIG. 12 depicts an image of LED die formed by various cleavings along different crystallographic planes, according to some embodiments. As an option, the present technique of cleaving along different crystallographic planes may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 12 shows the sidewall morphology for two LEDs on bulk GaN substrates which were cleaved with the same method but along two different crystal planes (a- and m-plane, as shown). The natural sidewall roughness obtained

in a-plane devices translates experimentally into higher light extraction efficiency. Such roughness is expected to increase light extraction by breaking the threefold in-plane symmetry of light propagation in the chip (e.g., by randomizing the azimuthal angle of propagation ϕ). FIG. 12 shows scanning electron microscope images of triangular chips cleaved along different crystallographic planes of a GaN substrate. The m-plane chip has relatively smooth sidewalls while the a-plane chip has pronounced one-dimensional roughness.

FIG. 21 shows the encapsulation gain measured experimentally on LEDs similar to those of FIG. 12, according to some embodiments.

FIG. 21 shows the encapsulation gain performance of devices cleaved with the same method but along two different crystal planes (a- and m-plane, as shown), similar to the devices of FIG. 12. Encapsulation gain is an indirect measure of extraction efficiency; a lower encapsulation gain indicates a higher extraction efficiency. FIG. 21 shows that a cleave along the a-plane, which produces deeper vertical roughness in the LED's sidewalls, leads to a lower encapsulation gain.

FIG. 13 is a chart showing light extraction as a function of varied polar and azimuthal angles for 1D roughened sidewall surfaces for a volumetric chip for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction as a function of varied polar and azimuthal angles for 1D roughened sidewall surfaces for a volumetric chip may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 13 shows how the angle-resolved extraction diagram of a chip is modified by randomizing the in-plane angles. Some quasi-guided trajectories are broken, resulting in larger extraction efficiency. As seen on FIG. 13 however, the polar propagation angles are not randomized (because the sidewall roughness is vertical, and thus does not break symmetry in the vertical direction) and some quasi-guided trajectories remain for intermediate angles. Another way to texture the sidewalls is to introduce a two-dimensional texture—e.g. to break the planarity of the sidewalls along two directions. FIG. 13 shows details of extraction vs. polar (q) and azimuthal (f) angles, for a volumetric chip with a triangular base (lateral dimension 380 μm , height 200 μm) with top surface roughness and 1D sidewall roughness. Due to randomization of (f), extraction is improved for some large angles. The six side extraction cones effectively become an “extraction ring”. Extraction is still limited at intermediate angles.

FIG. 14 is a chart showing light extraction as a function of varied polar and azimuthal angles for 2D roughened sidewall surfaces for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction as a function of varied polar and azimuthal angles for 2D roughened sidewall surfaces for a volumetric chip having a triangular base may be implemented in the context of the architecture and functionality of the embodiments described herein. FIG. 14 shows details of extraction vs. polar (q) and azimuthal (f) angles, for a volumetric chip with a triangular base (lateral dimension 380 μm , height 200 μm) with top surface roughness and 2D sidewall roughness. All angles are efficiently randomized, either by the top or the sidewall roughness, resulting in high extraction at all angles.

FIG. 14 shows the corresponding light extraction diagram. In such a case, both polar and azimuthal angles are randomized upon incidence on the textured sidewall, which can further increase light extraction. Extraction is substantially

improved over some embodiments following the light extraction model of FIG. 13, especially in certain angular domains.

FIG. 15 and FIG. 16 exemplify the improvement in extraction efficiency predicted by implementing 1-dimensional and 2-dimensional sidewall roughening. With the loss parameters chosen, the extraction efficiency for a chip with only top roughness is 70%. 1D and 2D sidewall roughness boost extraction to ~74% and ~82%, respectively.

FIG. 15 is a chart showing light extraction for 1D roughened sidewall surfaces as a function of sidewall skewing angle for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction for 1D roughened sidewall surfaces as a function of sidewall angle for a volumetric chip having a triangular base may be implemented in the context of the architecture and functionality of the embodiments described herein. FIG. 15 shows Cex vs. one-dimensional sidewall roughness (the x-axis of this plot is the average angle of the sidewalls with respect to planar sidewalls) for a GaN LED with a triangular base (lateral dimension 380 μm , height 2009 μm) and with top surface roughness.

FIG. 16 is a chart showing light extraction for 2D roughened sidewall surfaces as a function of sidewall angle for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction for 2D roughened sidewall surfaces as a function of sidewall angle for a volumetric chip having a triangular base may be implemented in the context of the architecture and functionality of the embodiments described herein. FIG. 16 shows Cex vs. two-dimensional sidewall roughness for a GaN LED with a triangular base (lateral dimension 380 μm , height 200 μm) and with top surface roughness.

In comparing the light extraction of FIG. 15 to the light extraction of FIG. 16, the improvements can be seen.

FIG. 17 is a chart showing light extraction under varied sidewall and top roughness for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction under varied sidewall and top roughness for a volumetric chip having a triangular base may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 17 shows a 2-dimensional map of expected improvement by combining surface roughness and 2D sidewall roughness, for a variety of scattering strengths. Typical top surface roughness obtained by chemical or PEC etching can be described by a scattering strength $f > 0.4$. Therefore, complementing such a top surface roughness with a moderate sidewall roughness $f > 0.15$ is sufficient to achieve optimal extraction. FIG. 17 shows Cex vs. sidewall and top roughness for a GaN LED with a triangular base (lateral dimension 380 μm , height 200 μm) and with 2-dimensional top and sidewall surface roughness.

In the following embodiments, “texturation” or “roughness” describes an optical surface which deviates from planarity. The roughness may be random, periodic (as in the case of a photonic crystal for instance) or pseudo-periodic. The roughness may be produced by a variety of means, including chemical etching, electro-chemical etching, photo-electro-chemical etching, patterning and dry etching, regrowth of semiconductor material over a patterned interface, roughness due to a sawing/cleaving/laser scribing singulation process.

In one embodiment, the singulation process (which may combine laser scribing, sawing and cleaving) produces sidewall roughness.

In one embodiment, the present method and device includes a gallium and nitrogen (e.g., GaN) containing substrate having roughened regions vertically oriented with respect to a pair of electrode faces. In an embodiment, the electrode faces are configured on a c-plane. Preferably, the substrate is separated by way of scribing, which occurs using a laser scribing process having a short wavelength laser. The beam ablates by pulsing electromagnetic radiation on selected portions of the gallium and nitrogen containing substrate. The beam scribes the substrate along the a-plane. Preferably, the streets between devices are configured from about 1 to about 30 microns, although there can be variations. Each of the scribe regions has a width of 5 to 10 microns. The scribe regions are formed using a UV laser configured with a 355 nm source and an output power of 30 to 300 milli-Watts, but can be others. The laser pulses are in the nano-second regime, e.g., 2-100 nanoseconds. The laser device and beam ablates a portion of the gallium and nitrogen containing material. The devices are later separated using a break process along the scribe lines causing formation of the roughened regions, which are substantially m-plane in characteristic and forms the vertically oriented facets. Each of the m-faces has width of a few microns, but can also be other dimension. Additionally, each of the facets has a peak region surrounded by troughs, when viewed from the c-plane direction. Optionally, the method subjects the scribe region to a selective etchant to remove any light absorbing slag material, which may be a by-product from the laser scribing process. Depending on the laser pulsing frequency, stage speed, and chemistry used for removing the by-product from the laser scribe process, a 2D roughness region with equal depth to the laser scribe can be created on the sidewalls of the device to greatly enhance light extraction. The selection of the chemistry for removal of the by-products is extremely important as some chemistry will tend to look for crystal plans and smooth out the region, while others induce roughness such as KOH. In some embodiments for creating 2D roughness regions, the process creates two distinct regions on the sidewalls.

In some embodiments, the same procedure as above is employed. However, the laser ablation process is sufficient to fully ablate the substrate and produce full device singulation, so that no subsequent breaking step is required. In such embodiments, the 2D roughness region created by the laser ablation covers a large fraction, up to the totality, of the sidewalls.

In some embodiments, the LED is made of bulk GaN and has the shape of a prism with a triangular base. The top surface and the sidewalls all display 2-dimensional roughness, with a roughness feature size on the order of 1-2 micron and a roughness surface coverage larger than 0.5.

In another embodiment, the LED is made of bulk GaN and has the shape of a prism with a triangular base. The top surface displays 2-dimensional roughness, with a roughness feature size on the order of 1-2 micron and a roughness surface coverage larger than 0.5. The sidewalls display vertical striations (1D roughness) with a characteristic distance of 1-5 μm .

FIG. 18 is a chart showing light extraction under varied substrate absorption for a volumetric chip having a triangular base for achieving high-performance light extraction from a Group III-nitride volumetric LED chip using surface and sidewall roughening. As an option, the present model for light extraction under varied substrate absorption for a volumetric

chip having a triangular base may be implemented in the context of the architecture and functionality of the embodiments described herein.

FIG. 18 describes the impact of absorption coefficient on extraction efficiency. The Group III-nitride substrate has a crystal orientation such that its sidewalls can easily be roughened. FIG. 18 shows Cex vs. GaN substrate absorption for a triangular chip (lateral dimension 380 μm , height 200 μm) with top surface roughness.

According to some embodiments:

Only some of the sidewalls are roughened.

The sidewalls are slanted and roughened.

The LED is grown on a bulk Group III-nitride substrate, and the resulting vertical-to-horizontal aspect ratio of the LED chip is larger than 5%.

The LED is grown on a foreign substrate, but the Group III-nitride layer is thick enough that the vertical-to-horizontal aspect ratio of the LED chip is larger than 5%.

The absorption coefficient of the Group III-nitride film is lower than 10 cm^{-1} , than 1 cm^{-1} .

FIG. 19 shows a light emitting diode device having a top surface region with a textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm; and a lateral surface region having a textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm. As an option, the present light emitting diode device may be implemented in the context of the architecture and functionality of the embodiments described herein. Or, the present light emitting diode device or any characteristic therein may be preset in any desired environment. FIG. 19 shows a light emitting diode device having n-type material overlying an active region, in turn overlying p-type epitaxial material. An n-contact is coupled to the n-type epitaxial material and a p-contact is coupled to the p-type epitaxial material. The top surface region has a textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm; and at least one lateral surface region having a textured surface characterized by a surface roughness of about 80 nm to about 10,000 nm.

FIG. 20 shows light extraction as a function of roughness, according to some embodiments. Application of the surprising results as shown in FIG. 20 yields a technique for fabricating a light emitting diode device having roughened regions. Strictly as an example, fabricating a light emitting diode device having roughened regions can commence by providing a gallium and nitrogen containing substrate including a top surface region, a lateral surface region, an n-type epitaxial material overlying a portion of the top surface region. One or more active regions can be formed overlying the n-type epitaxial material, and p-type epitaxial material disposed to overlie the one or more active regions. Then, a first electrode can be coupled to the n-type epitaxial material (or the substrate material), and a second electrode coupled to the p-type epitaxial material.

FIG. 20 shows performance for surface-roughened LEDs where the typical feature size of the roughness is varied. As observed in FIG. 20, increasing the feature size beyond 1 μm leads to an improvement in performance. This can be justified by considering scattering theory: scattering features smaller than the wavelength of light (e.g., $\sim 400\text{ nm}$) are in the Rayleigh scattering regime, where scattering increases with feature size. This leads to the trend observed on FIG. 20. This trend is expected to saturate as features become larger than 1 μm and scattering enters a geometric regime. Therefore, FIG. 20 suggests minimum feature sizes for a good surface roughness. Feature sizes larger than 1 μm provide the best scatter-

ing, while feature sizes in the range 100 nm-1 μ m provide a decent, although non-optimal, range.

Likewise, there is a practical maximum for the feature size which is desirable. Features of tens or hundreds of microns become comparable with the overall shape of the LED and can be impractical to form and handle. Therefore, the range 1 μ m-10 μ m may be considered a preferred range because it leads to good scattering and is practical.

Various techniques can be used to form singulation regions, and various techniques can be used for separating at the singulation region boundaries. Optimizing said techniques can improve the roughness, and hence the extraction efficiency.

FIG. 22 compares SEM images of LED devices obtained by two singulation techniques. As an option, such techniques be implemented in the context of the architecture and functionality of the embodiments described herein.

The devices in FIG. 22 were singulated by using a laser scribing process followed by a breaking process. The two devices employed two methods. Each method uses a different laser profile during the laser scribing. Method 1 uses a multiple-beam profile; method 2 uses a single-beam profile. Due to the successive effect of the multiple beams as they are rastered along the scribing line, method 1 produces a strong 2-dimensional roughness in the laser-ablated region. Method 1, on the other hand, produces a moderate 2-dimensional roughness.

In general, the parameters of the laser scribing process (such as the beam profile, rastering, pulse width and power) may be optimized to enhance the roughness in the laser-ablated region.

FIG. 23 compares the lumen output performance of white LEDs whose LED chips were obtained by two singulation techniques, as shown on FIG. 22. FIG. 23 shows that the LED produced by method 1 leads to a higher lumen output.

FIG. 24 is a sketch of the laser beam profile of a laser-ablation tool. Such a profile may be used for fabricating embodiments of the invention. FIG. 24 shows a laser beam profile composed of several (here, four) beams. This multiple-beam profile is rastered across the singulation direction. Thanks to the rastering, the same area of the semiconductor is illuminated several times by one of the beams. This can lead to a more pronounced roughness.

Some specifications according to some embodiments:

Vertical-to-horizontal chip aspect ratio >5%.

Average lateral size of rough features between 1 μ m and 10 μ m.

Average vertical size of rough features between 100 nm and 10 μ m.

Average surface coverage of 2-dimensional rough features: top surface >0.5, sidewall >0.15.

A combination of sidewall and surface roughness, such that for any polar angle at least one of the surfaces has a one-bounce extraction efficiency into the outside medium larger than 10%.

Base shape of the LED can be a square, a triangle, a parallelogram.

The absorption coefficient of the Group III-nitride film is lower than 10 cm^{-1} . The embodiment of FIG. 18 describes the impact of absorption coefficient on extraction efficiency. Alternatively, some embodiments are characterized where the product of the typical chip dimension, and of the substrate coefficient, is smaller than 0.1 This can be understood to mean that the typical absorption through one light bounce in the chip will be less than 10%.

According to an embodiment, the present disclosure relates to a technique where the side roughness is formed by cleaving sawing the chip.

According to an embodiment, the present disclosure relates to a technique where the side roughness is formed by chemical or PEC etching.

According to an embodiment, the present disclosure relates to a technique where the side roughness is formed by patterning and dry etching of the chip.

According to an embodiment, the present disclosure relates to a technique where the side roughness is formed by separation of the devices by laser ablation of the material inbetween, followed by etching of the laser process by-products inducing a 2D roughness on the crystalline face of the device.

According to an embodiment, the present disclosure relates to a technique where the side roughness is formed by depositing a film (such as a dielectric) on the side of the LED and texturing it.

According to an embodiment, the present disclosure relates to a technique where slanted sidewalls are formed by laser scribing with multiple beams.

According to an embodiment, the present disclosure relates to a technique where a Group III-nitride layer is grown on a foreign substrate (and possibly separated from the foreign substrate) such that the vertical-to-horizontal aspect ratio of the Group III-nitride layer is at least 5%, and LEDs with top and sidewall roughness are formed.

According to an embodiment, the present disclosure relates to a technique where a layer of a Group III-nitride substrate is separated from the rest of the substrate such that the vertical-to-horizontal aspect ratio of the resulting Group III-nitride layer is at least 5%, and LEDs with top and sidewall roughness are formed.

In one embodiment, a plurality of light emitting diode devices is provided overlying a bulk-GaN containing substrate. Through suitable fabrication steps, a plurality of p-type metallic ohmic contacts is provided overlying the p-type GaN layer of the light emitting diode device structure, as part of the embodiment. Additionally, a plurality of n-type ohmic contacts is provided overlying the n-type GaN layer of the light emitting diode device structure, as part of the embodiment.

In an embodiment, the plurality of light emitting diode devices is singulated into individual chips using wafer sawing or dicing, where the wafer sawing or dicing induces a surface texture or roughness on the sidewalls of the singulated light emitting diode chips, where the surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip. In one embodiment, a suitable wet chemical etching step may be applied after the wafer sawing or dicing step, so as to form a second texture or roughness characterizing the plurality of surfaces exposed to the wet etching step, where the second surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip.

In another embodiment, the plurality of light emitting diode devices is singulated into individual chips using laser scribing followed by breaking, where the laser scribing induces a surface texture or roughness on the sidewalls of the singulated light emitting diode chips, where the surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip. In an particular embodiment, a suitable wet chemical etching step may be applied between the laser scribing and breaking steps, in order to remove the slag formed as a result of the laser scribing, and this wet etching step may

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result in a second texture or roughness characterizing the plurality of surfaces exposed to the wet etching step, where the second surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip.

In another embodiment, the plurality of light emitting diode devices are singulated into individual chips by fully ablating the substrate material between devices utilizing a laser. The laser ablation process induces a rough surface of slag and crystalline material on the side faces of the chips. The slag material can be etch away to prevent light absorption and retain only the roughness from the crystalline material. Alternatively, the slag itself can be used as a mask in conjunction with etching to imprint the roughness on the crystalline material followed by the removal of the slag material.

In another embodiment, the plurality of light emitting diode devices is singulated into individual chips using diamond scribing and breaking, where the diamond scribing and breaking step induces a surface texture or roughness on the sidewalls of the singulated light emitting diode chips, where the surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip. In an embodiment, the diamond scribing and breaking may be performed along a direction or a plurality of directions which are substantially misaligned with respect to a crystalline direction or a plurality of crystalline directions of the GaN-containing substrate.

In another embodiment, the diamond scribing and breaking may be performed along a direction or plurality of directions which are substantially aligned with respect to a crystalline direction or plurality of crystalline directions of the GaN-containing substrate.

In yet another embodiment, the plurality of light emitting diode devices is singulated into individual chips using diamond scribing and breaking. In this embodiment, a suitable wet chemical etching step may be applied between the diamond scribing and breaking steps, so as to form a second texture or roughness characterizing the plurality of surfaces exposed to the wet etching step, where the second surface texture or roughness has a characteristic pattern, pitch or shape which enhances the extraction of light from the light emitting diode chip.

In an embodiment, the diamond scribing and breaking may be performed along a direction or a plurality of directions which are substantially misaligned with respect to a crystalline direction or a plurality of crystalline directions of the GaN-containing substrate. Alternatively, the diamond scribing and breaking may be performed along a direction or plurality of directions which are substantially aligned with respect to a crystalline direction or plurality of crystalline directions of the GaN-containing substrate. That is, the scribing is performed along at least one direction or a plurality of directions that are substantially misaligned with respect to a crystalline direction or a plurality of crystalline directions plane of the gallium and nitrogen containing substrate. In an embodiment, the direction is substantially misaligned is within ± 5 or ± 10 or ± 20 degrees of the plane of the gallium and nitrogen containing substrate. As used herein, the term misaligned is provided intentionally and is generally an off-set or the like. Depending upon the embodiment, the plane of the gallium and nitrogen containing substrate is one of a plurality of planes of the substrate material selected from a group consisting of at least c-plane, m-plane, or a-plane or others and their combinations, and semipolar planes. Again, there can be other variations, modifications, and alternatives.

In an embodiment, the characteristic texture or roughness may be substantially dissimilar across the plurality of sur-

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faces formed as a result of the light emitting diode device singulation process. In yet another embodiment, the characteristic texture or roughness may be substantially similar across the plurality of surfaces formed as a result of the light emitting diode device singulation process.

In an embodiment, no specific means or methods are applied to apply a surface texture or roughness to the surface or plurality of surfaces of the light emitting diode device chip which are overlaid by the p-type metallic contact or n-type metallic contact or both. In another embodiment, means or methods are applied to apply a surface texture or roughness to the surface or plurality of surfaces of the light emitting diode device chip which are overlaid by the p-type metallic contact or n-type metallic contact or both.

The foregoing description of the exemplary embodiments has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to enable others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly, the scope of the present invention is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

What is claimed is:

1. A light emitting diode comprising:
 - a gallium and nitrogen containing substrate comprising a surface region;
 - an n-type epitaxial material overlying the surface region;
 - one or more active regions overlying the n-type epitaxial material;
 - a p-type epitaxial material overlying the one or more active regions;
 - a first electrode coupled to the n-type epitaxial material, to the substrate, or to both the n-type epitaxial material and to the substrate;
 - a second electrode coupled to the p-type epitaxial material; and
 - at least three lateral surface regions extending from a top surface of the light emitting diode to a base of the light emitting diode;
 - wherein at least one of the at least three lateral surface regions comprises a first portion characterized by a one-dimensional surface roughness.
2. The light emitting diode of claim 1, wherein the one-dimensional surface roughness is characterized by striations extending from the top surface toward the base.
3. The light emitting diode of claim 1, wherein the one-dimensional surface roughness is characterized by an average lateral size from 1 μm to 10 μm .
4. The light emitting diode of claim 1, wherein the one-dimensional surface roughness is characterized by an average vertical size from 100 nm and 10 μm .
5. The light emitting diode of claim 1, wherein the first portion extends from the top surface toward the base.
6. The light emitting diode of claim 1, wherein the at least one of the at least three lateral surface regions comprises a second portion extending from the first portion to the base.
7. The light emitting diode of claim 1, wherein the at least three lateral surface regions comprise an a-plane surface.

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8. The light emitting diode of claim 1, wherein the top surface comprises a surface roughness.

9. The light emitting diode of claim 1, wherein the light emitting diode is characterized by a vertical to horizontal aspect ratio from 1:20 to 1:1.

10. The light emitting diode of claim 1, wherein the light emitting diode has the shape of a prism with a triangular base.

11. The light emitting diode of claim 1, wherein the at least three lateral surface regions are at an angle with respect to the top surface and the base.

12. The light emitting diode of claim 1, wherein, the top surface is triangular;

the base is triangular; and

the at least three lateral surface regions comprise three lateral surface regions.

13. The light emitting diode of claim 1, wherein the light emitting diode has a thickness from 5 μm to 20 μm .

14. The light emitting diode of claim 1, wherein the one-dimensional surface roughness is configured to extract a substantial portion of electromagnetic radiation derived from the one or more active regions.

15. The light emitting diode of claim 1, wherein the one or more active regions comprises two or more of indium, gallium, aluminum, and nitrogen.

16. The light emitting diode of claim 1, wherein the at least one lateral surface region is configured in a non-polar orientation.

17. The light emitting diode of claim 1, wherein the at least one lateral surface region is configured in a semi-polar orientation.

18. The light emitting diode of claim 1, wherein the at least one lateral surface region is configured in a polar orientation.

19. The light emitting diode of claim 1, wherein the at least one lateral surface region is misaligned with a crystallographic plane of the gallium and nitrogen containing substrate.

20. The light emitting diode of claim 1, wherein the at least one lateral surface region is misaligned within ± 20 degrees with respect to a crystallographic plane of the gallium and nitrogen containing substrate.

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21. The light emitting diode of claim 2, wherein the striations are characterized by a distance of 1 μm to 5 μm .

22. The light emitting diode of claim 6, wherein the second portion is characterized by a two-dimensional surface roughness.

23. The light emitting diode of claim 8, wherein the surface roughness ranges from about 80 nm to about 10,000 nm.

24. The light emitting diode of claim 8, wherein the top surface roughness is configured to extract a substantial portion of electromagnetic radiation derived from the one or more active regions.

25. The light emitting diode of claim 11, wherein the angle is from 1 degrees to 20 degrees.

26. The light emitting diode of claim 22, wherein the two-dimensional surface roughness is characterized by a feature size on the order of 1 μm to 2 μm .

27. The light emitting diode of claim 22, wherein the two-dimensional surface roughness ranges from about 80 nm to about 10,000 nm.

28. A light emitting diode comprising:
 a gallium and nitrogen containing substrate comprising a surface region;
 an n-type epitaxial material overlying the surface region;
 one or more active regions overlying the n-type epitaxial material;
 a p-type epitaxial material overlying the one or more active regions;
 a first electrode coupled to the n-type epitaxial material, to the substrate, or to both the n-type epitaxial material and to the substrate;
 a second electrode coupled to the p-type epitaxial material;
 a triangular top surface comprising a top textured surface;
 a triangular base; and
 three lateral surface regions extended from the top surface to the base,
 wherein a portion of each of the three lateral surface regions is characterized by a one-dimensional surface roughness.

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