US009484431B1

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 9,484,431 B1**
(45) **Date of Patent: Nov. 1, 2016**

(54) **PURE BORON FOR SILICIDE CONTACT**

(71) Applicant: **International Business Machines Corporation**, Armonk, NY (US)

(72) Inventors: **Chia-Yu Chen**, White Plains, NY (US); **Zuoguang Liu**, Schenectady, NY (US); **Sanjay C. Mehta**, Niskayuna, NY (US); **Tenko Yamashita**, Schenectady, NY (US)

(73) Assignee: **INTERNATIONAL BUSINESS MACHINES CORPORATION**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/812,399**

(22) Filed: **Jul. 29, 2015**

(51) **Int. Cl.**

H01L 29/00	(2006.01)
H01L 29/66	(2006.01)
H01L 21/768	(2006.01)
H01L 21/3065	(2006.01)
H01L 21/225	(2006.01)
H01L 29/417	(2006.01)
H01L 29/49	(2006.01)
H01L 29/51	(2006.01)
H01L 29/78	(2006.01)
H01L 21/311	(2006.01)
H01L 29/167	(2006.01)
H01L 29/08	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/665*** (2013.01); ***H01L 21/2251*** (2013.01); ***H01L 21/3065*** (2013.01); ***H01L 21/31111*** (2013.01); ***H01L 21/76831*** (2013.01); ***H01L 21/76877*** (2013.01); ***H01L 29/0847*** (2013.01); ***H01L 29/167*** (2013.01); ***H01L 29/41725*** (2013.01); ***H01L 29/495*** (2013.01); ***H01L 29/516*** (2013.01); ***H01L 29/517*** (2013.01); ***H01L 29/78*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/0847; H01L 29/167; H01L 29/41725; H01L 29/795; H01L 29/516; H01L 29/517; H01L 29/78
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,860,085	A *	8/1989	Feygenson	H01L 29/42304 257/513
4,868,631	A *	9/1989	Hollingsworth	H01L 21/763 257/517
5,242,847	A	9/1993	Ozturk et al.	
5,281,552	A	1/1994	King et al.	
5,721,148	A *	2/1998	Nishimura	H01L 29/1087 148/DIG. 126
6,406,962	B1 *	6/2002	Agnello	H01L 21/84 257/E21.703

(Continued)

OTHER PUBLICATIONS

Mohammadi, V., et al.; "An Analytical Kinetic Model for Chemical-Vapor Deposition of PureB Layers From Diborane"; Journal of Applied Physics; vol. 112; pp. 113501-1-113501-10; 2012.

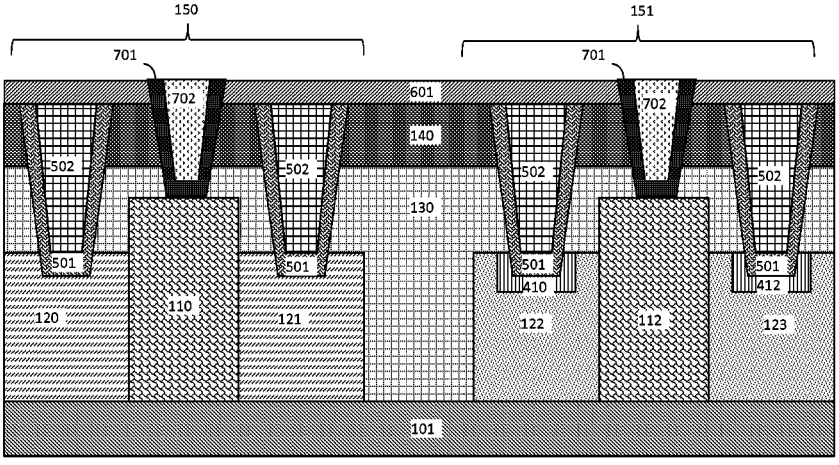
(Continued)

Primary Examiner — Ida M Soward
(74) *Attorney, Agent, or Firm* — Cantor Colburn LLP; Vazken Alexanian

(57) **ABSTRACT**

A semiconductor device includes a gate disposed over a substrate; a source region and a drain region on opposing sides of the gate; and a pair of trench contacts over and abutting an interfacial layer portion of at least one of the source region and the drain region; wherein the interfacial layer includes boron in an amount in a range from about 5×10^{21} to about 5×10^{22} atoms/cm^2.

7 Claims, 11 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

6,627,502	B1 *	9/2003	Cho	H01L 21/2257 257/E21.151
6,797,602	B1	9/2004	Kluth et al.	
6,873,017	B2 *	3/2005	Cai	H01L 29/7833 257/355
8,617,938	B2	12/2013	De Souza et al.	
8,642,471	B2 *	2/2014	Yin	H01L 29/66545 257/288
8,901,537	B2	12/2014	Murthy et al.	
9,884,104		3/2015	Glass et al.	
9,318,603	B2 *	4/2016	Su	H01L 29/7827
9,324,831	B2 *	4/2016	Zschatzsch	H01L 29/66545
2008/0160697	A1 *	7/2008	Kao	H01L 29/41741 438/268
2009/0020808	A1 *	1/2009	Yu	H01L 21/28525 257/330
2010/0264488	A1 *	10/2010	Hsieh	H01L 29/1095 257/334
2011/0006362	A1 *	1/2011	Hsieh	H01L 29/1095 257/330
2011/0266638	A1 *	11/2011	Frohberg	H01L 21/28518 257/412
2011/0272765	A1 *	11/2011	Seo	H01L 23/485 257/410
2012/0146090	A1 *	6/2012	Lui et al.	H01L 29/8613 257/139
2012/0171817	A1 *	7/2012	Hebert	H01L 21/82348 438/107
2013/0146953	A1 *	6/2013	Cheng	H01L 21/84 257/296
2013/0230948	A1	9/2013	Scheiper et al.	
2013/0240990	A1 *	9/2013	Yin	H01L 29/456 257/343
2014/0131796	A1 *	5/2014	Zhou	H01L 29/66681 257/336
2014/0199837	A1 *	7/2014	Hung	H01L 21/76816 438/675
2014/0284710	A1 *	9/2014	Hossain	H01L 29/36 257/330
2014/0306290	A1 *	10/2014	Alptekin	H01L 29/41725 257/369
2016/0104673	A1 *	4/2016	Tung	H01L 23/5226 257/288

OTHER PUBLICATIONS

Sarubbi, Francesco; "Characterization of Pure Boron Depositions Integrated in Silicon Diodes for Nanometer-Deep Junction Applications"; Tu Delft, Delft University of Technology; p. 1-122; 2010.

Sarubbi, Francesco, et al.; "Chemical Vapor Deposition of α-Boron Layers on Silicon for Controlled Nanometer-Deep p+n. Junction Formation"; Journal of Electronic Materials; vol. 39, No. 2; p. 162-173; 2010.

* cited by examiner

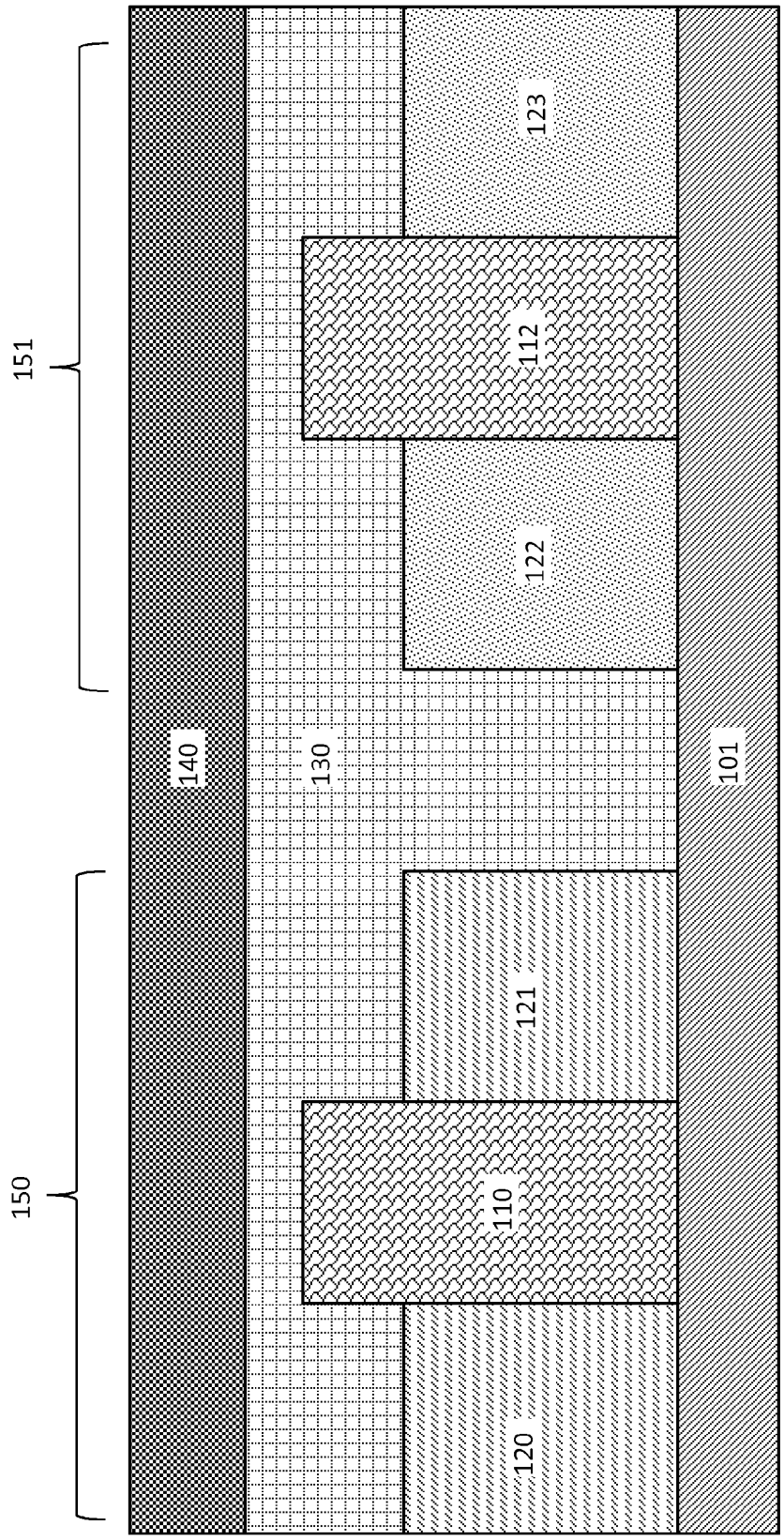


FIG. 1

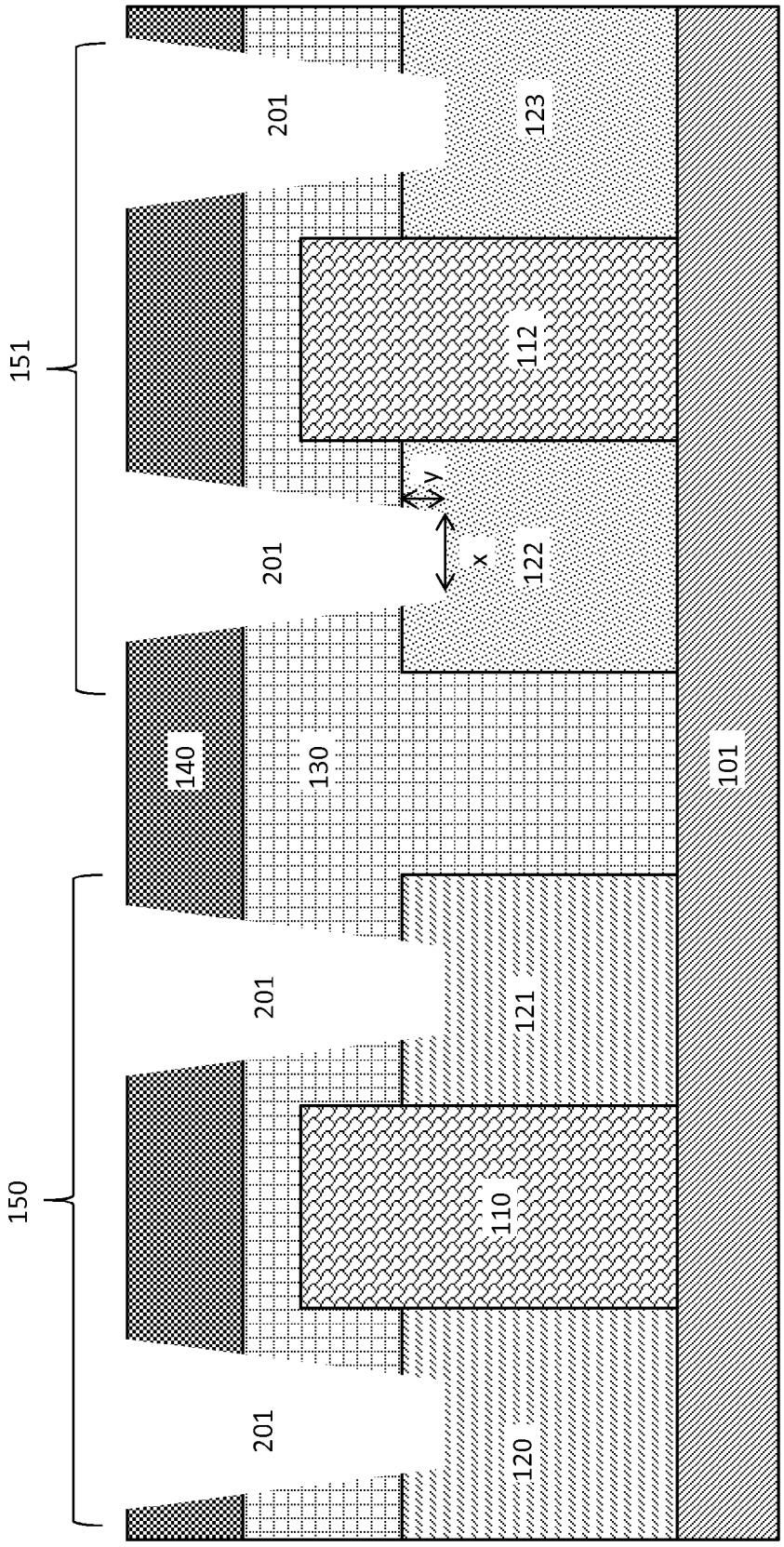


FIG. 2

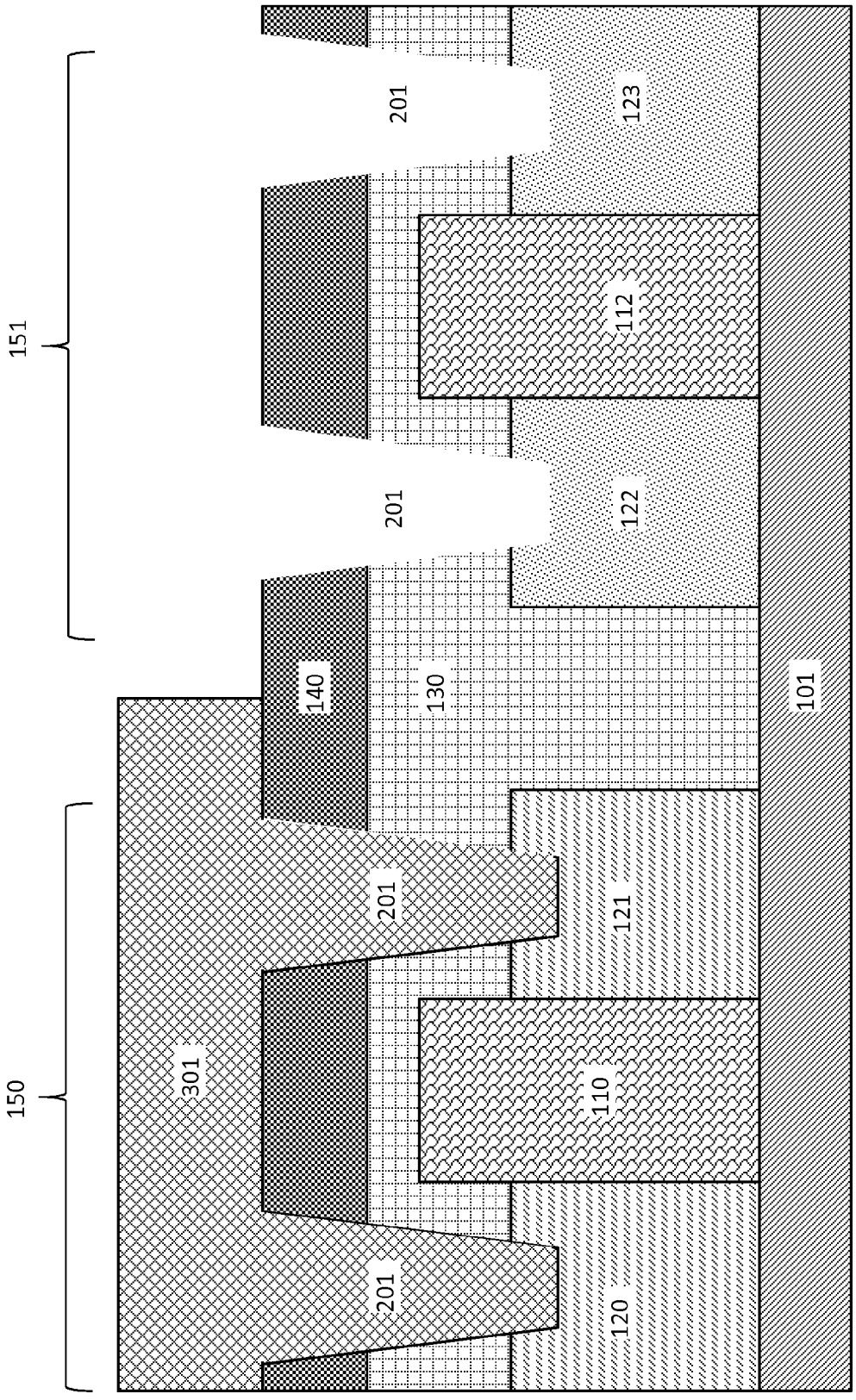


FIG. 3

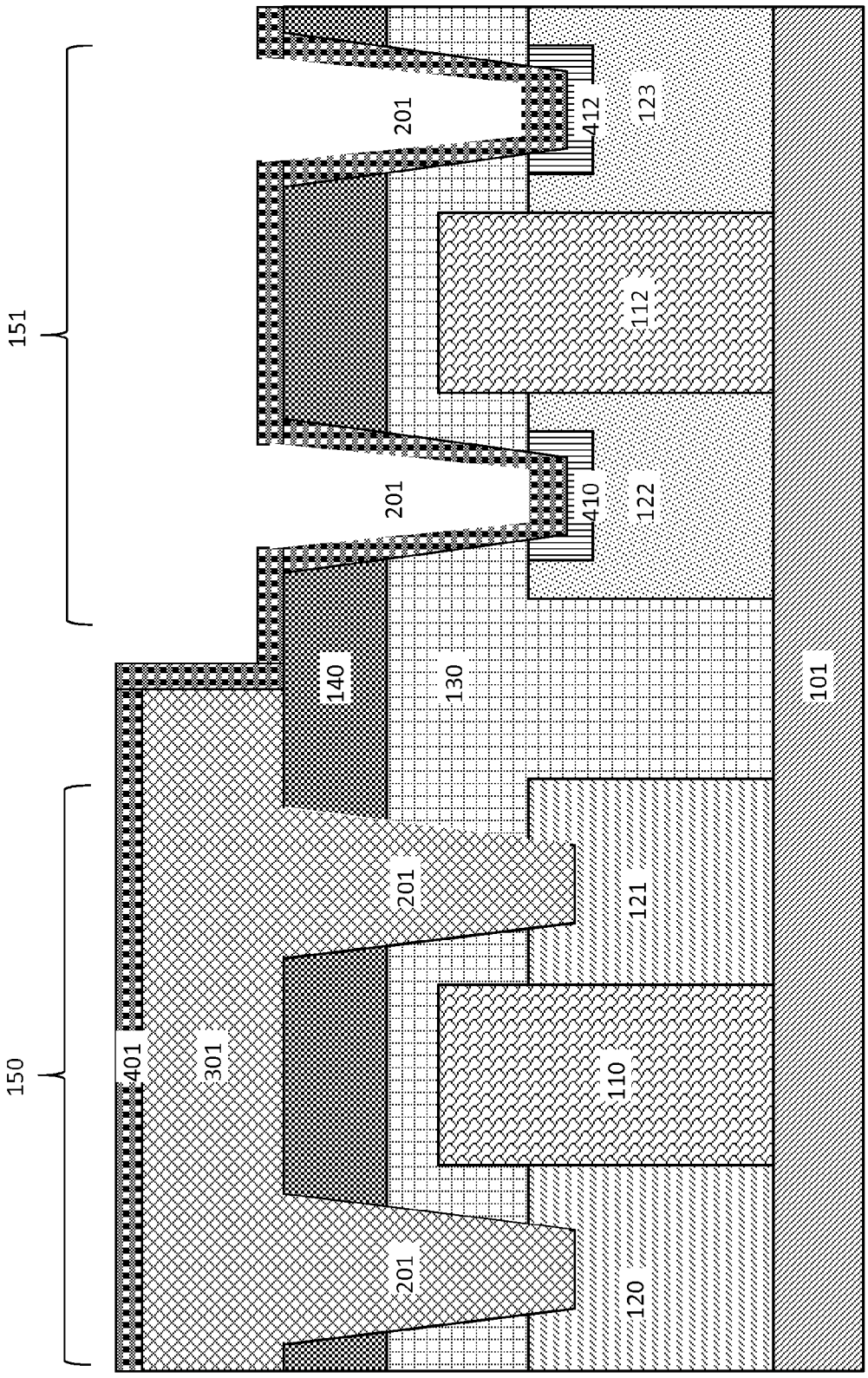

151
150
201
412
123
112
201
410
122
140
130
101
201
121
401
301
110
201
120

FIG. 4A

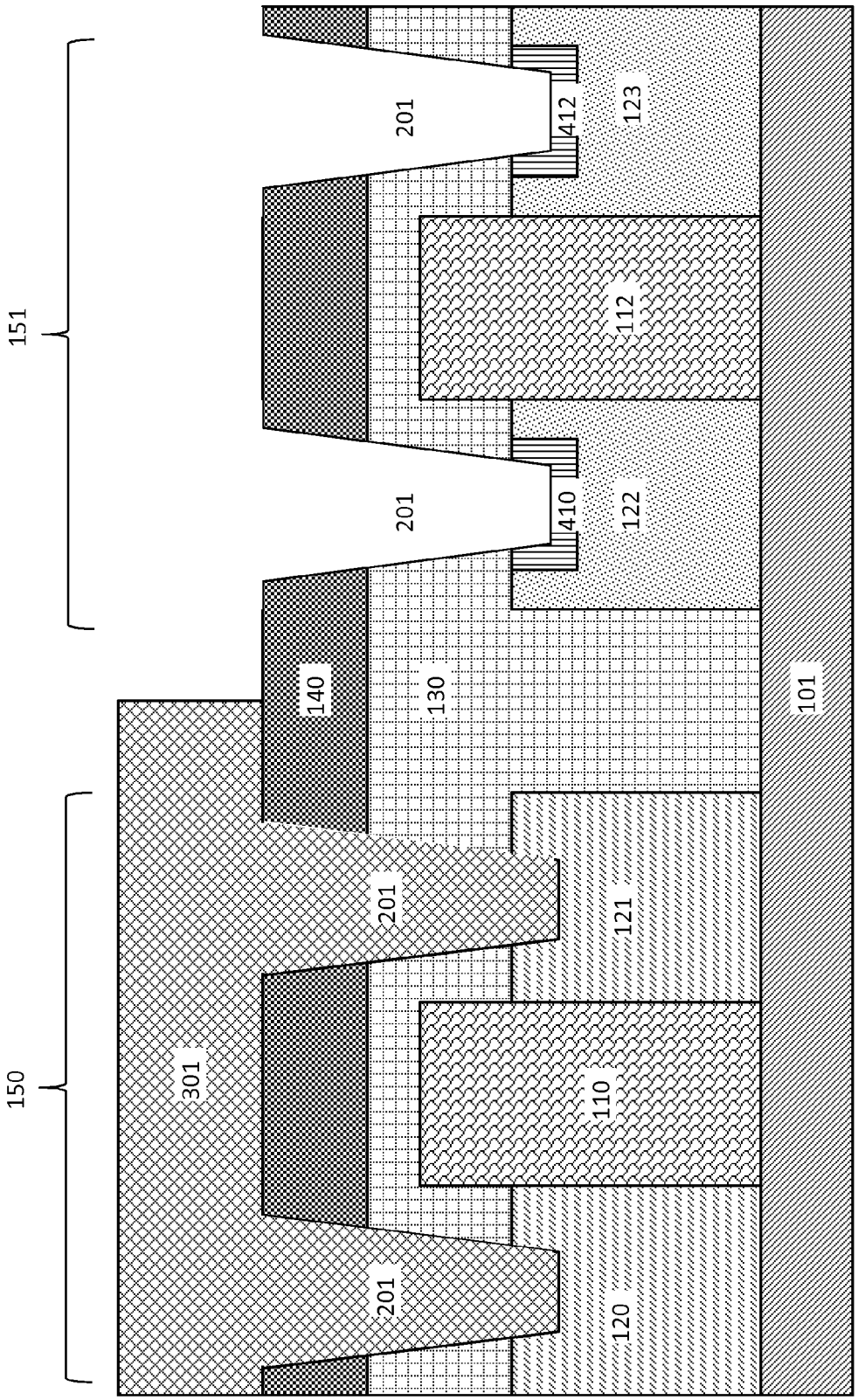

151
150
201
412
123
112
201
410
122
140
130
101
201
121
301
110
201
120

FIG. 4B

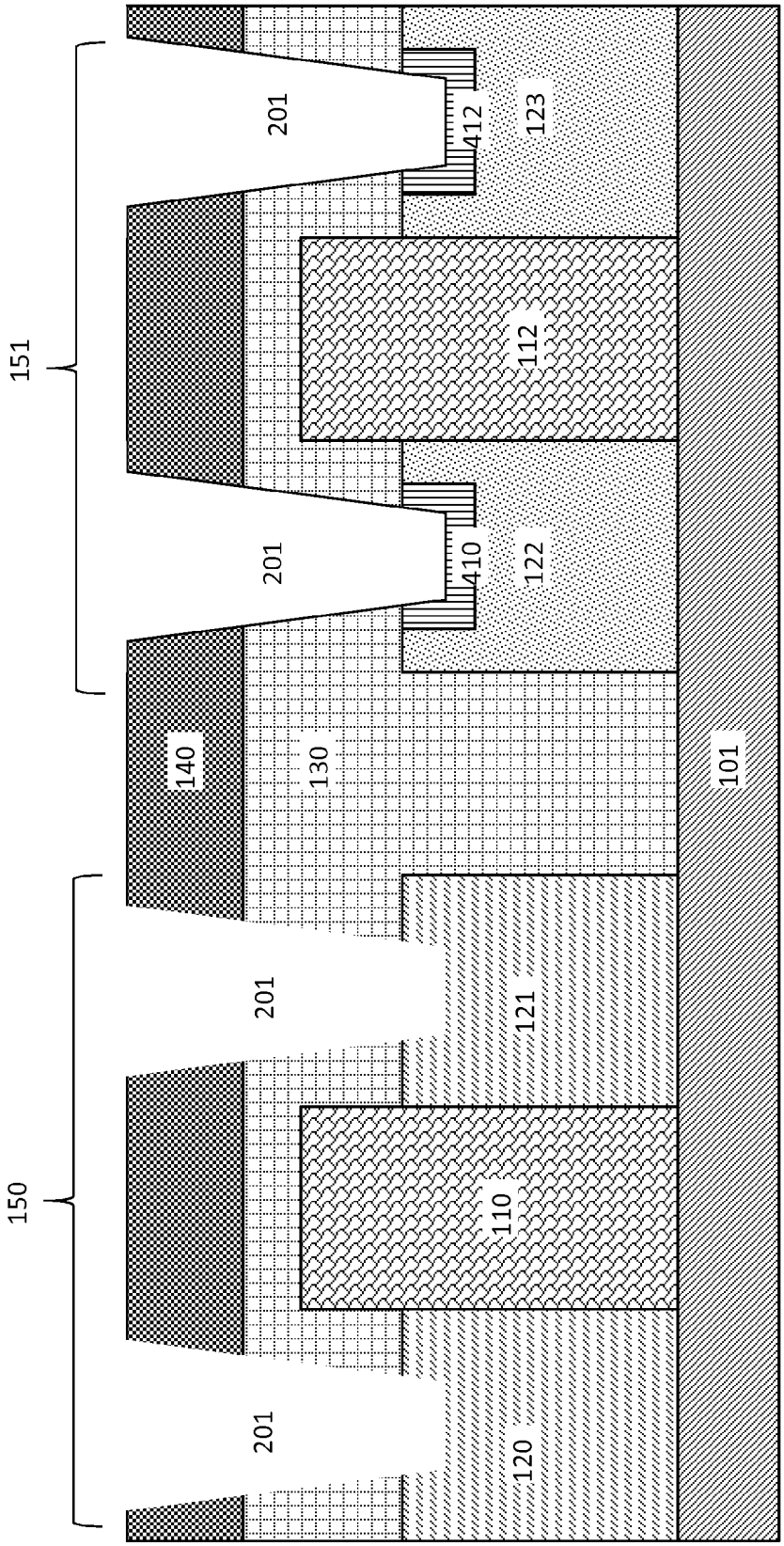


FIG. 4C

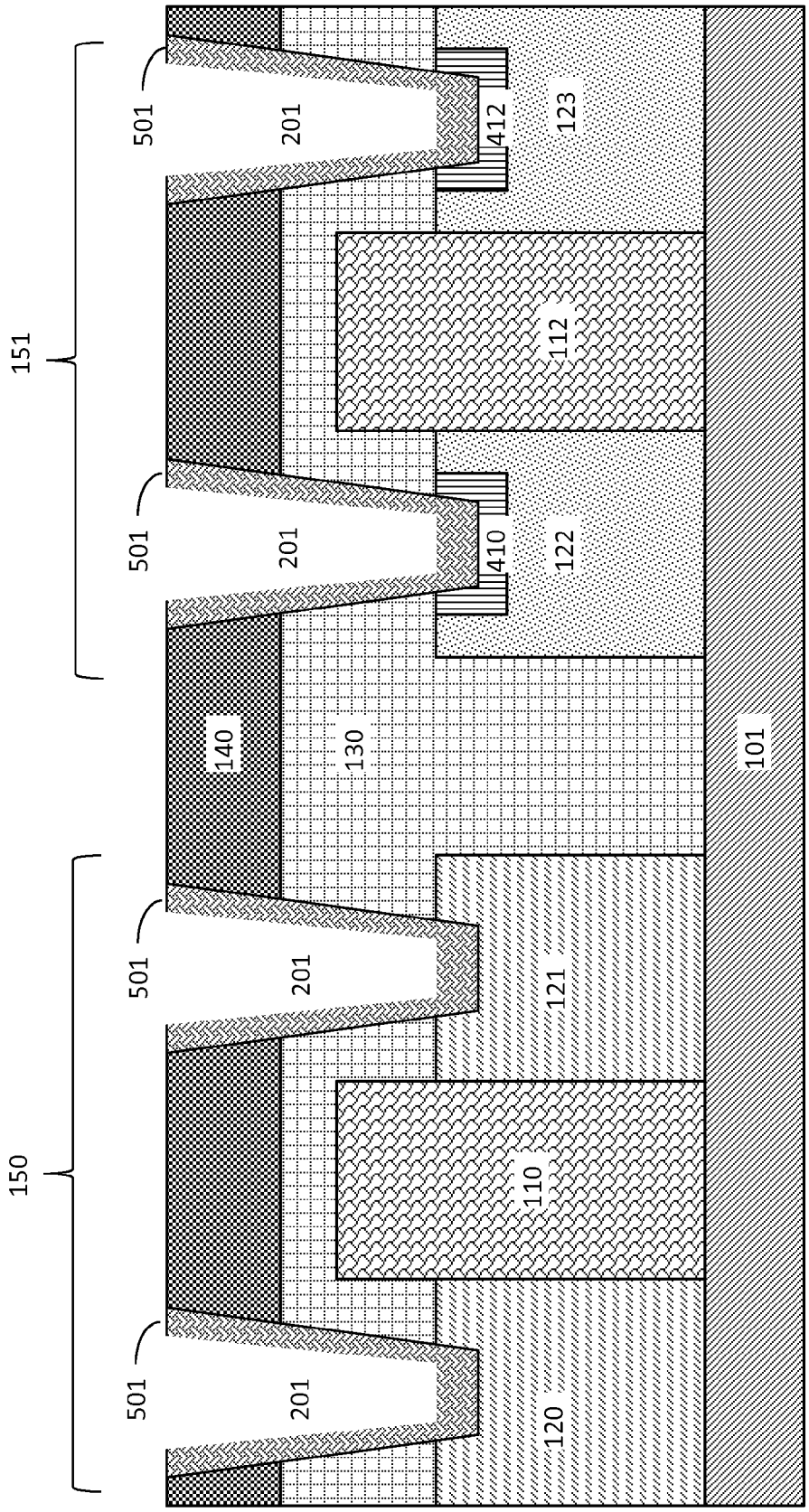


FIG. 5A

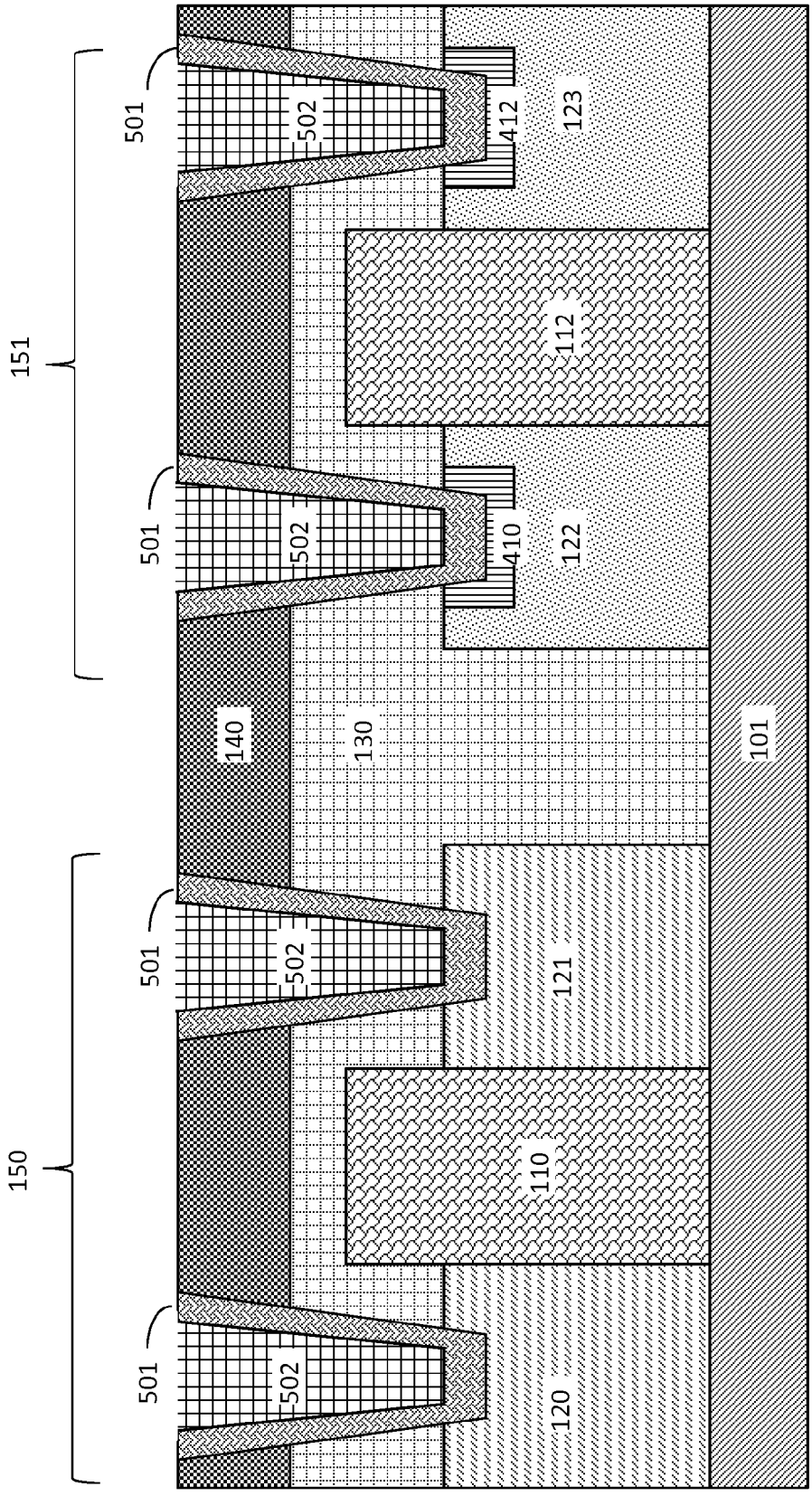


FIG. 5B

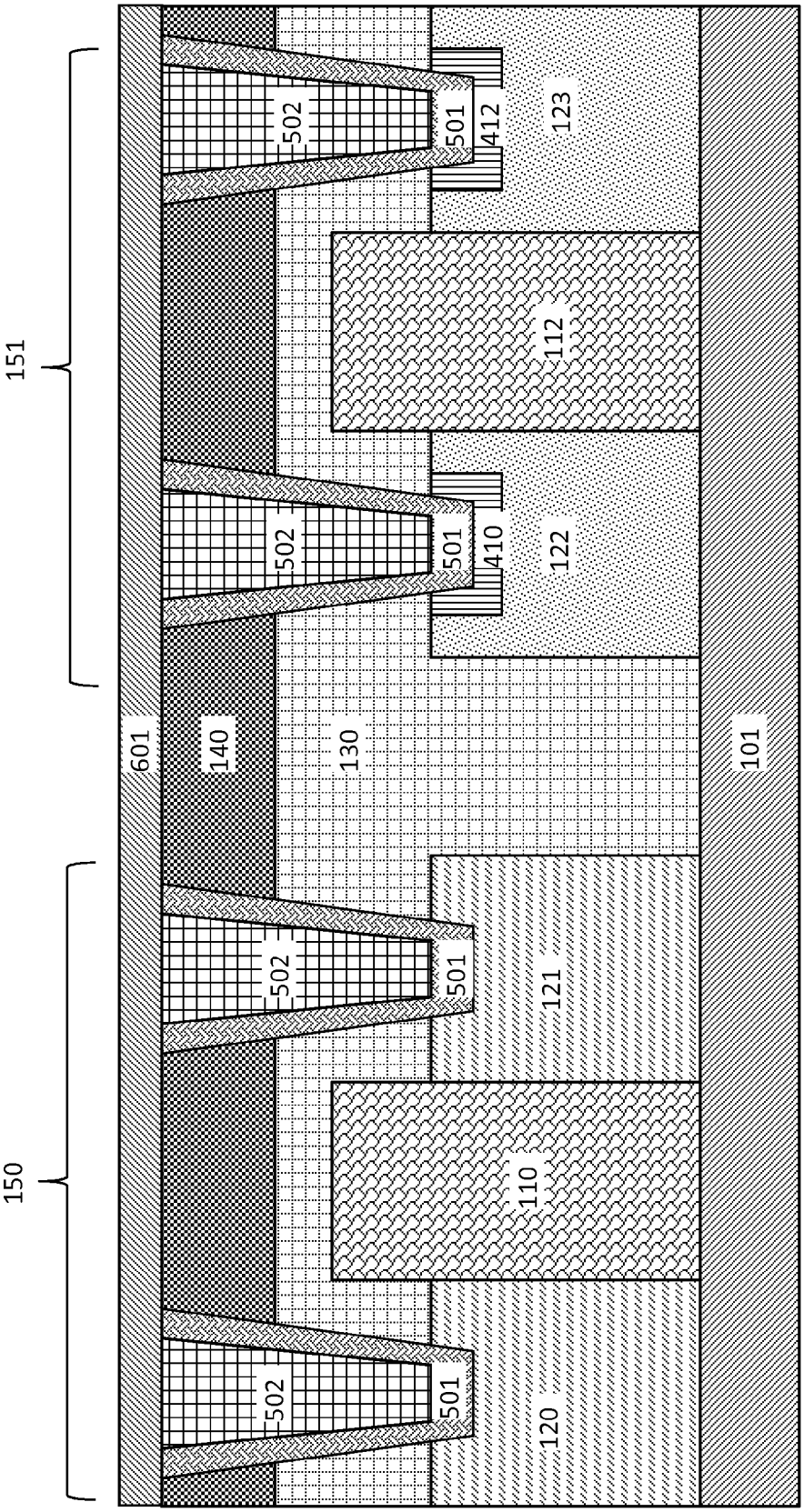


FIG. 6A

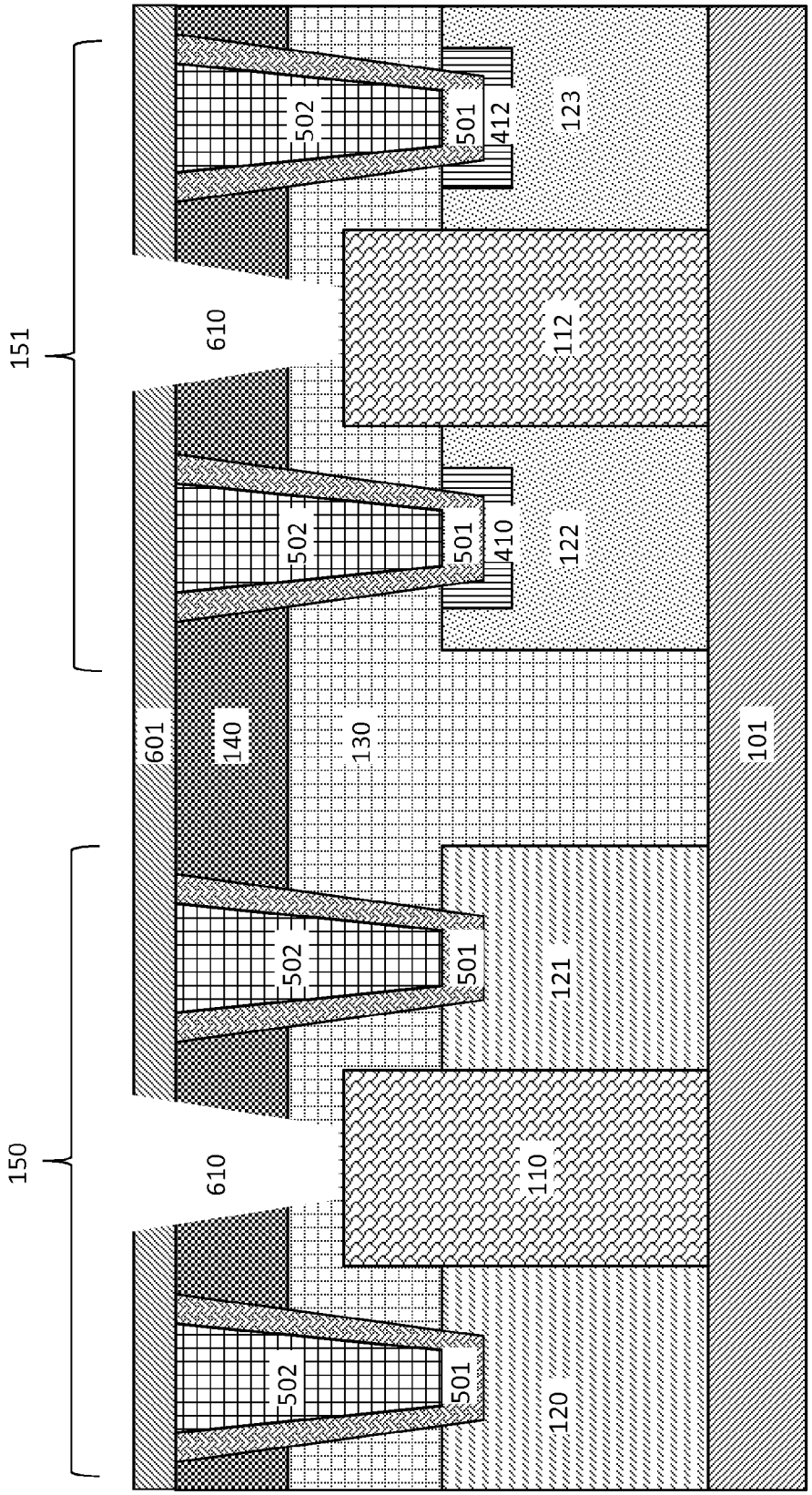

151
150
610
610
601
140
130
101
502
501
412
123
112
502
501
410
122
502
501
121
110
502
501
120

FIG. 6B

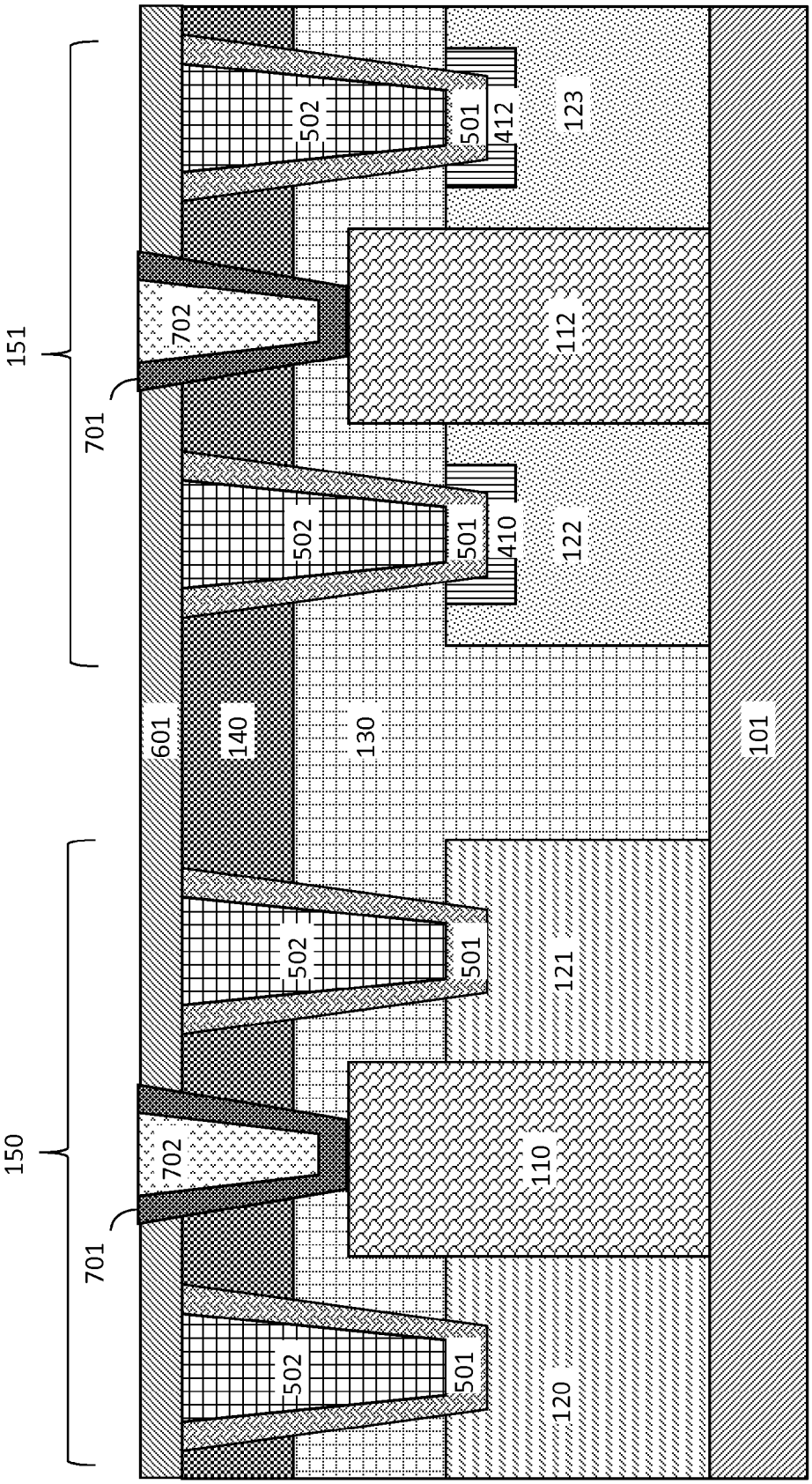

151
150
701
701
702
702
502
502
502
502
501
501
501
501
412
410
123
122
121
120
112
110
601
140
130
101

FIG. 7

PURE BORON FOR SILICIDE CONTACT

BACKGROUND

The present invention generally relates to metal-oxide-semiconductor field-effect transistors (MOSFET), and more specifically, to source/drain contact structures.

The MOSFET is a transistor used for amplifying or switching electronic signals. The MOSFET has a source, a drain, and a metal oxide gate electrode. The metal gate is electrically insulated from the main semiconductor n-channel or p-channel by a thin layer of insulating material, for example, silicon dioxide or glass, which makes the input resistance of the MOSFET relatively high. The gate voltage controls whether the path from drain to source is an open circuit ("off") or a resistive path ("on").

N-type field effect transistors (NFET) and p-type field effect transistors (PFET) are complementary MOSFETs. The NFET uses electrons as the majority current carriers and is built directly on a p-type substrate with n-doped source and drain junctions (also called epitaxial contacts) and an n-doped gate. The PFET uses holes as the majority current carriers and is built on an n-well with p-doped source and drain junctions (epitaxial contacts) and a p-doped gate. The dopant concentration in the source and drain junctions is an important parameter for optimal transistor function.

SUMMARY

In one embodiment of the present invention, a semiconductor device includes a gate disposed over a substrate; a source region and a drain region on opposing sides of the gate; and a pair of trench contacts over and abutting an interfacial layer portion of at least one of the source region and the drain region; wherein the interfacial layer includes boron in an amount in a range from about 5×10^{21} to about 5×10^{22} atoms/cm^2.

In another embodiment, a method of making a semiconductor device includes performing an epitaxial growth process to form epitaxial contacts on opposing sides of a gate positioned over a substrate; removing portions of the epitaxial contacts to form trench contact patterns; depositing a conformal layer including amorphous boron within the trench contact patterns, the conformal layer forming a discrete interfacial layer within the epitaxial contacts, and the discrete interfacial layer including boron in an amount in a range from about 5×10^{21} to about 5×10^{22} atoms/cm^2; removing the conformal layer including amorphous boron; and filling the trench contact patterns with a high-k dielectric material and a conductive metal to form the trench contacts.

Yet, in another embodiment, a method of making a semiconductor device includes performing an epitaxial growth process to form epitaxial contacts on opposing sides of a gate positioned over a substrate; removing portions of the epitaxial contacts to form trench contact patterns; performing a deposition process to deposit a conformal layer including substantially pure amorphous boron within the trench contact patterns, the conformal layer forming a discrete interfacial layer within the epitaxial contacts comprising boron in an amount in a range from about 5×10^{21} to about 5×10^{22} atoms/cm^2; removing the conformal layer including amorphous boron; and filling the trench contact patterns with a high-k dielectric material and a conductive metal to form the trench contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIGS. **1-7** illustrate an exemplary method of making a PFET source/drain contact according to embodiments the present invention, in which:

FIG. **1** is a cross-sectional side view of a semiconductor device with a PFET and a NFET formed over a substrate;

FIG. **2** is a cross-sectional side view after performing an etching process to form trench contacts over the source/drain regions;

FIG. **3** is a cross-sectional side view after lithographic patterning to block the NFET region;

FIG. **4**A is a cross-sectional side view after depositing a conformal layer of amorphous boron;

FIG. **4**B is a cross-sectional side view after removing the amorphous boron layer;

FIG. **4**C is a cross-sectional side view after removing the lithographic patterning mask;

FIG. **5**A is a cross-sectional side view after depositing a liner in the trench contacts;

FIG. **5**B is a cross-sectional side view after filling the trench contact with a conductive metal;

FIG. **6**A is a cross-sectional side view after depositing an oxide layer over the semiconductor device;

FIG. **6**B is a cross-sectional side view after etching to form the gate contact patterns over the gates; and

FIG. **7** is a cross-sectional side view after depositing a gate contact liner and conductive gate material.

DETAILED DESCRIPTION

Although the dopant concentration (e.g., boron (B) concentration) can significantly improve functioning at the PFET source/drain contact, the ability to increase the dopant concentration by ion implantation or other methods (e.g., in-situ based doping) is limited to an upper limit of about 5×10^{20} atoms/centimeter^2 (atoms/cm^2).

Accordingly, embodiments of the present invention provide a PFET source/drain contact with a high boron concentration in silicon (Si) or silicon germanium (SiGe), up to about 3×10^{22} atoms/cm^2. Further, the boron mixes with the Si or SiGe with to provide high activity in the contact because a high boron concentration provides decreased resistance. A method of making the PFET source/drain contact with a high boron concentration (e.g., 1×10^{19} to about 1×10^{21} atoms/cm^2) is now described in detail with accompanying figures. It is noted that like reference numerals refer to like elements across different embodiments.

The following definitions and abbreviations are to be used for the interpretation of the claims and the specification. As used herein, the terms "comprises," "comprising," "includes," "including," "has," "having," "contains" or "containing," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a composition, a mixture, process, method, article, or apparatus that comprises a list of elements is not necessarily limited to only those elements but can include other elements not expressly listed or inherent to such composition, mixture, process, method, article, or apparatus.

As used herein, the articles "a" and "an" preceding an element or component are intended to be nonrestrictive regarding the number of instances (i.e. occurrences) of the element or component. Therefore, "a" or "an" should be read to include one or at least one, and the singular word form of

the element or component also includes the plural unless the number is obviously meant to be singular.

As used herein, the terms "invention" or "present invention" are non-limiting terms and not intended to refer to any single aspect of the particular invention but encompass all possible aspects as described in the specification and the claims.

As used herein, the term "about" modifying the quantity of an ingredient, component, or reactant of the invention employed refers to variation in the numerical quantity that can occur, for example, through typical measuring and liquid handling procedures used for making concentrates or solutions. Furthermore, variation can occur from inadvertent error in measuring procedures, differences in the manufacture, source, or purity of the ingredients employed to make the compositions or carry out the methods, and the like. In one aspect, the term "about" means within 10% of the reported numerical value. In another aspect, the term "about" means within 5% of the reported numerical value. Yet, in another aspect, the term "about" means within 10, 9, 8, 7, 6, 5, 4, 3, 2, or 1% of the reported numerical value.

Turning now to the Figures, FIGS. **1-7** illustrate an exemplary method of making a PFET source/drain contact according to embodiments of present invention. FIG. **1** is a cross-sectional side view of a semiconductor device with a NFET **150** and a PFET **151** formed over a common substrate **101**. Non-limiting examples of suitable substrate materials include silicon, silicon dioxide, aluminum oxide, sapphire, germanium, gallium arsenide (GaAs), an alloy of silicon and germanium, indium phosphide (InP), or any combination thereof. Other examples of suitable substrates **101** include silicon-on-insulator (SOI) substrates with buried oxide (BOX) layers. The thickness of the substrate **101** is not intended to be limited. In one aspect, the thickness of the substrate **101** is in a range from about 2 mm to about 6 mm for bulk semiconductor substrates. In another aspect, the thickness of the substrate **101** is in a range from about 25 nm to about 50 nm for the silicon layer in SOI substrates

To form the epitaxial contacts forming the source regions **120** and **122** and the drain region **121** and **123**, lithography and etching are performed. Lithography can include depositing a photoresist (not shown) onto the substrate **101** and developing the exposed photoresist with a resist developer to provide a patterned photoresist. The epitaxial contacts are formed by performing an epitaxial growth process to deposit a doped material (e.g., silicon). The type of dopant used depends on whether the MOSFET is the NFET **150** or the PFET **151**. Non-limiting examples of suitable dopants for the NFET **150** include n-type dopants (e.g., Group V elements such as phosphorus). Non-limiting examples of suitable dopants for the PFET **151** include p-type dopants (e.g., Group III such as boron). Generally, the concentration of dopant in the epitaxial contacts is in a range from about 1×10^{19} to about 1×10^{21} atoms/cm^2.

The thickness of the epitaxial contacts forming the source regions **120** and **122** and the drain regions **121** and **123** is not intended to be limited. In one aspect, the thickness of the epitaxial contacts is in a range from about 5 nm to about 60 nm. In another aspect, the thickness of the epitaxial contacts is in a range from about 5 nm to about 10 nm.

The gates **110** and **112** are formed by lithographic patterning and etching. Initially, a "dummy gate" is formed by filling the gate region with a suitable removable gate material, for example, amorphous silicon (polysilicon). The removable gate material is subsequently removed, and the gates **110** and **112** are filled with a conductive gate material. A high-k dielectric liner can be deposited before filling with the conductive gate material.

The high-k dielectric material can be a dielectric material having a dielectric constant greater than 4.0, 7.0, or 10.0. Non-limiting examples of suitable materials for the high-k dielectric material include oxides, nitrides, oxynitrides, silicates (e.g., metal silicates), aluminates, titanates, nitrides, or any combination thereof. Other non-limiting examples of suitable high-k dielectric materials include HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, Y_2O_3, a pervoskite oxide, or any combination thereof. The high-k dielectric material layer may be formed by known deposition processes, for example, chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), evaporation, physical vapor deposition (PVD), chemical solution deposition, or other like processes. The thickness of the high-k dielectric material may vary depending on the deposition process as well as the composition and number of high-k dielectric materials used. The high-k dielectric material layer may have a thickness in a range from about 0.5 to about 20 nm.

Non-limiting examples of suitable conductive gate metals include aluminum (Al), platinum (Pt), silver (Au), tungsten (W), titanium (Ti), or any combination thereof. The conductive metal may be deposited by a known deposition process, for example, CVD, PECVD, PVD, plating, thermal or e-beam evaporation, and sputtering.

The thickness of the gates **110** and **112** is not intended to be limited. In one aspect, the thickness of the gates **110** and **112** is in a range from about 20 nm to about 75 nm. In another aspect, the thickness of the gates **110** and **112** is in a range from about 20 nm to about 50 nm.

A blanket oxide layer **130** is deposited onto both NFET **150** and PFET **151** regions over the substrate **101**. Non-limiting examples of suitable materials for the oxide layer **130** include flowable oxides (e.g., liquid solutions of hydrogen silsesquioxane in a carrier solvent) and silicon dioxide. The thickness of the oxide layer **130** is not intended to be limited. In one aspect, the thickness of the oxide layer **130** is in a range from about 50 nm to about 150 nm. In another aspect, the thickness of the oxide layer **130** is in a range from about 60 nm to about 115 nm.

An optional silicon nitride (SiN) layer **140** is deposited onto the oxide layer **130**. The thickness of the SiN layer **140** is not intended to be limited. In one aspect, the thickness of the SiN layer **140** is in a range from about 5 nm to about 20 nm. In another aspect, the thickness of the SiN layer **140** is in a range from about 10 nm to about 15 nm.

FIG. **2** is a cross-sectional side view after performing an etching process to form trench contacts **201** over the source regions **120** and **122** and drain regions **121** and **123**. The etching process may be a dry etching process, for example, reactive ion etching (RIE). The etching process is performed through the SiN layer **140**, the oxide layer **130**, and a portion of the epitaxial contacts of the source regions **120** and **122** and drain regions **121** and **123**. The etching process removes a portion of and stops within a region of the epitaxial contacts to form a recess. The open trench contacts **201** form a trench contact pattern. The trench contact patterns have side walls (y) and a base (x) that protrude into the epitaxial contacts of the source region **122** and the drain region **123**.

FIG. **3** is a cross-sectional side view after lithographic patterning to block the NFET **150** region. A hard mask layer **301** is deposited over the NFET **150** portion of the substrate **110**. The hard mask layer **301** may include, for example, amorphous carbon (a-C), silicon nitride (SiN), or silicon

dioxide (SiO_2). The hard mask layer **301** fills the open regions of the trench contacts **201**.

FIG. **4**A is a cross-sectional side view after depositing a conformal layer of amorphous boron. The amorphous boron layer **401** is formed by using a deposition process (e.g., CVP or ALD) to deposit a conformal layer of amorphous boron within the trench contacts **201** over the PFET **151**. The amorphous boron layer **401** includes substantially pure boron. In one embodiment, the amorphous boron layer **401** includes 100 atomic % (at. %) boron. In another embodiment, the amorphous boron layer **401** includes at least 99 at. % boron. Yet, in another embodiment, the amorphous boron layer **401** includes at least 98 at. % boron.

Deposition of the amorphous boron layer **401** may be performed by Chemical Vapor Deposition (CVD). The conditions of the CVD process may be tailored to the particular semiconductor device. The CVD process may be performed at atmospheric pressure (i.e., about 760 Torr), or reduced pressures, for example 60 Torr or 36 Torr. In one exemplary embodiment, the deposition is performed at processing temperatures ranging from about 500° C. to about 800° C. Diborane (B_2H_6) is injected into the reactor chamber as the dopant gas at a flow rate of, for example, 490 standard cubic centimeters per minute (sccm). Hydrogen gas (H_2) may be used as the carrier gas and for dilution of the doping source.

The hard mask layer **301** protects the trench contacts **201** over the NFET **150** region. The amorphous boron layer **401** lines the trench contacts **201** of the PFET **151** and forms an interfacial layer **410** including a high boron concentration in the epitaxial contacts of the source region **122** and drain region **123**. The interfacial layer **410** naturally forms in the source region **122** and drain region **123** upon disposing amorphous boron layer **401** within the trench contacts **201**.

In one aspect, the interfacial layer **410** has a thickness in a range from about 0.5 nm to about 2 nm. In another aspect, the interfacial layer **410** has a thickness in a range from about 1 nm to about 1.5 nm. Yet, in another aspect, the interfacial layer **410** has a thickness about or in any range from about 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, and 1.5 nm.

In one aspect, the interfacial layer **410** has a boron concentration in a range from about 5×10^{21} to about 5×10^{22} atoms/cm^2. In another aspect, the interfacial layer **410** has a boron concentration in a range from about 1×10^{22} to about 3×10^{22} atoms/cm^2.

FIG. **4**B is a cross-sectional side view after removing the amorphous boron layer **401**. The amorphous boron layer **401** may be removed using any suitable process. Although the amorphous boron layer **401** is stripped, the interfacial layer **410** remains over the source region **122** and the drain region **123**. In one non-limiting example, a boiling solution of concentrated nitric acid (HNO_3) is used to remove the amorphous boron layer **401**. The temperature of the HNO_3 can be, for example, 110° Celsius (° C.). The concentration of the HNO_3 can be, for example, between about 50 and about 85%. In another non-limiting example, an aqua regia process can be used to remove the amorphous boron layer **401**. An aqua regia process involves using a nitro-hydrochloric acid (HCl) to etch away the amorphous boron layer **401**. The nitro-HCl mixture is formed by mixing concentrated nitric acid and hydrochloric acid in a volume ratio of, for example, 1:3.

FIG. **4**C is a cross-sectional side view after removing the hard mask layer **301** over the NFET **150** region. The hard mask layer **301** can be removed by a wet cleaning process using, for example, HF or HCl and dry etching. Suitable dry etching processes include RIE, plasma etching, ion beam etching, laser ablation, or any combination thereof.

FIG. **5**A is a cross-sectional side view after depositing a liner **501** in the trench contacts **201**. To form the liner **501**, a high-k dielectric material is deposited into the trench contacts. The high-k dielectric material can be a dielectric material having a dielectric constant greater than 4.0, 7.0, or 10.0. Non-limiting examples of suitable materials for the high-k dielectric material include oxides, nitrides, oxynitrides, silicates (e.g., metal silicates), aluminates, titanates, nitrides, or any combination thereof. Other non-limiting examples of suitable high-k dielectric materials include HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, Y_2O_3, a pervoskite oxide, or any combination thereof. The high-k dielectric material layer may be formed by known deposition processes, for example, CVD, PECVD, ALD, evaporation, PVD, chemical solution deposition, or other like processes. The thickness of the high-k dielectric material may vary depending on the deposition process as well as the composition and number of high-k dielectric materials used.

In one embodiment, the liner **501** includes a bilayer of Ti and TiN. The TiN is deposited over the layer of Ti to form the Ti/TiN liner. The thickness of the liner **501** can generally vary and is not intended to be limited. In one aspect, the thickness of the liner **501** is in a range from about 3 nm to about 10 nm. In another aspect, the thickness of the liner **501** is in a range from about 4 nm to about 9 nm.

FIG. **5**B is a cross-sectional side view after filling the trench contacts **201** with a conductive metal **501**. Non-limiting examples of suitable conductive metals include tungsten, aluminum, platinum, gold, or any combination thereof. A planarization process, for example chemical mechanical planarization (CMP), is performed over the conductive metal **501**. The conductive metal may be deposited by a known deposition process, for example, CVD, PECVD, PVD, plating, thermal or e-beam evaporation, and sputtering.

FIG. **6**A is a cross-sectional side view after depositing a blanket oxide layer **601** over the NFET **150** and PFET **151** regions of the semiconductor device. The oxide layer **601** can include, for example, tetraethyl-ortho-silicate (TEOS) or silicon dioxide.

FIG. **6**B is a cross-sectional side view after etching to form the gate contact patterns **610** over the gates **110** and **112**. In one non-limiting example, a RIE process is performed to form the gate contact patterns **610**.

FIG. **7** is a cross-sectional side view after depositing a gate contact liner **701** and conductive gate material **702** into the gate contact patterns **610**. The gate contact liner **701** can include, for example, a high-k dielectric material as described above for liner **501** (see FIG. **5**A). The conductive gate material **702** can be any of the conductive metal materials described above for the trench contacts **201** (see FIG. **5**B). A planarization process, for example, a CMP process, is performed over the conductive gate material **702**.

The above described embodiments of semiconductor devices and methods of making such devices provide various advantages. The methods provide a PFET source/drain contact with a high boron concentration in Si or SiGe, up to about $3\text{-}5\times10^{22}$ atoms/cm^2. After depositing a layer of amorphous boron over the source and drain a contact, the boron mixes with the Si or SiGe with to provide high activity in the contact.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms

as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, element components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

The flow diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the spirit of the invention. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed is:

1. A semiconductor device, comprising:

a gate disposed over a substrate;

a source region and a drain region on opposing sides of the gate; and

a pair of trench contacts over and abutting an interfacial layer portion of at least one of the source region and the drain region, the trench contacts having sidewalls and a base, and both the sidewalls and the base contacting the interfacial layer;

wherein the interfacial layer comprises boron in an amount in a range from about 5×1021 to about 5×1022 atoms/cm^2.

2. The semiconductor device of claim **1**, wherein the pair of trench contacts is positioned within a recessed region of epitaxial contacts.

3. The semiconductor device of claim **1**, wherein the interfacial layer has a thickness in a range from about 0.5 to about 2 nanometers (nm).

4. The semiconductor device of claim **1**, wherein the semiconductor device is a p-type field effect transistor (PFET).

5. A semiconductor device, comprising:

a gate disposed over a substrate;

a source region and a drain region on opposing sides of the gate; and

a pair of trench contacts over and abutting an interfacial layer portion of at least one of the source region and the drain region, the pair of trench contacts comprising a high-k dielectric material and a conductive metal;

wherein the interfacial layer comprises boron in an amount in a range from about 5×1021 to about 5×1022 atoms/cm^2.

6. The semiconductor device of claim **5**, wherein the high-k dielectric material contacts the interfacial layer.

7. The semiconductor device of claim **5**, wherein the conductive metal is tungsten, aluminum, platinum, gold, or any combination thereof.

* * * * *