



US009270907B2

(12) **United States Patent**  
Naito et al.

(10) **Patent No.:** US 9,270,907 B2  
(45) **Date of Patent:** Feb. 23, 2016

(54) **RADIATION IMAGING APPARATUS,  
CONTROL METHOD FOR RADIATION  
IMAGING APPARATUS, AND STORAGE  
MEDIUM**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 814 days.

(21) Appl. No.: **13/237,354**

(22) Filed: **Sep. 20, 2011**

(65) **Prior Publication Data**  
US 2012/0087471 A1 Apr. 12, 2012

(30) **Foreign Application Priority Data**  
Oct. 12, 2010 (JP) ..... 2010-230102

(51) **Int. Cl.**  
**H04N 5/341** (2011.01)  
**H04N 5/357** (2011.01)  
**H04N 5/32** (2006.01)  
**H04N 5/345** (2011.01)  
**H04N 5/374** (2011.01)

(Continued)

(52) **U.S. Cl.**  
CPC ..... **H04N 5/357** (2013.01); **H04N 5/32** (2013.01); **H04N 5/341** (2013.01); **H04N 5/345** (2013.01); **H04N 5/378** (2013.01); **H04N 5/3742** (2013.01); **H04N 5/37452** (2013.01)

(58) **Field of Classification Search**  
USPC ..... 250/370.09  
See application file for complete search history.

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*Primary Examiner* — David Porta

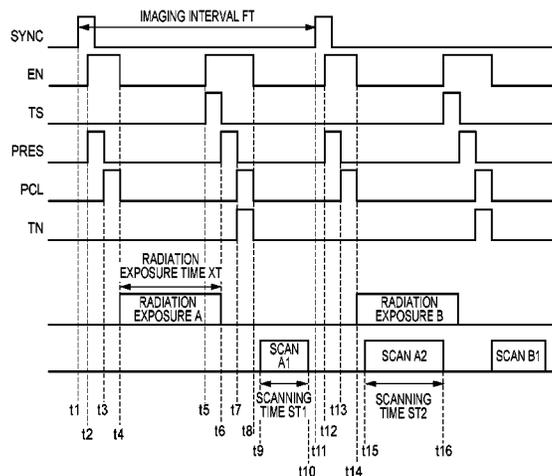
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(57) **ABSTRACT**

A radiation imaging apparatus including an accumulation unit to accumulate electrical charge in accordance with radiation for each pixel circuit of a plurality of pixel circuits. An output unit outputs an analog signal for each pixel circuit by sampling and holding an electrical signal in accordance with a voltage of an accumulation unit for each pixel circuit. The output unit stops the output during a reset operation of the accumulation unit. A selection unit selects pixel circuits that output the analog signals. The selection unit stops the selection during a reset operation of the accumulation unit. A determination unit determines whether a total time of an exposure time and an output time required to output the analog signals corresponding to all the pixel circuits is longer than an imaging interval that is based on a synchronization signal representing a radiation generation timing input from an external apparatus.

**11 Claims, 7 Drawing Sheets**



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FIG. 1

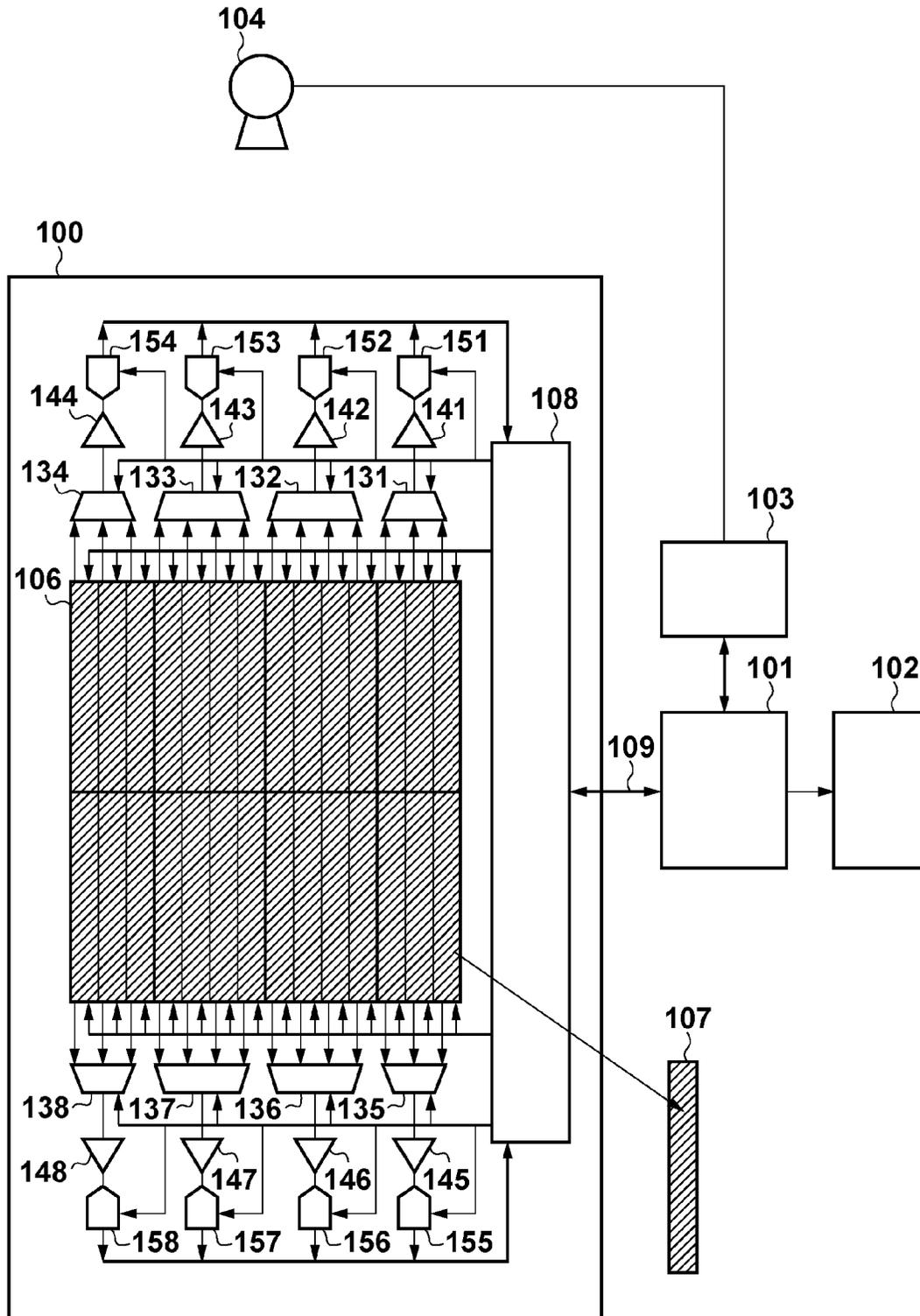




FIG. 4

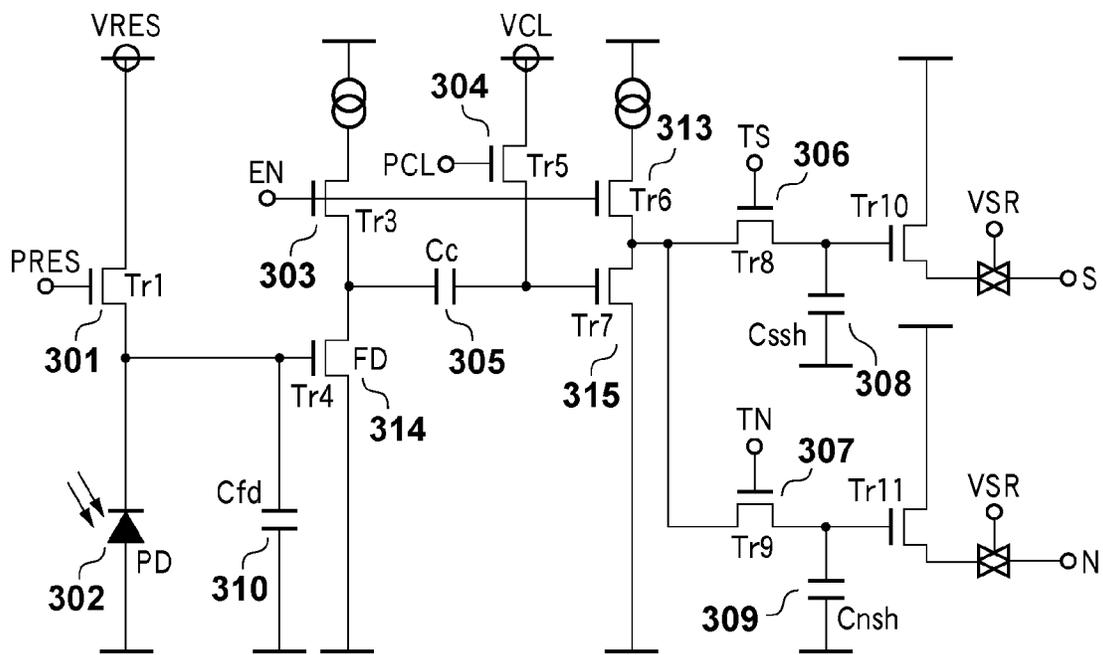


FIG. 5A

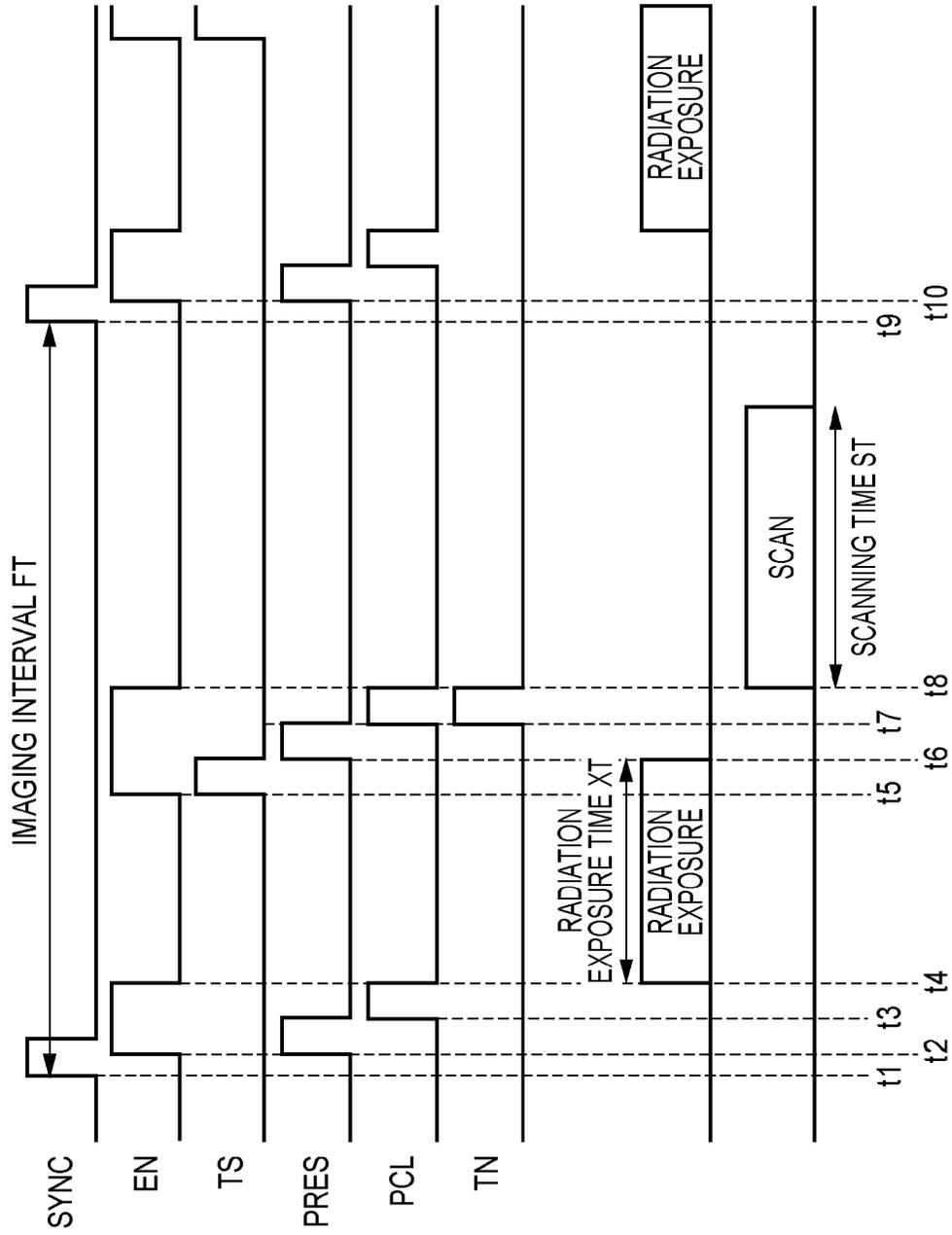
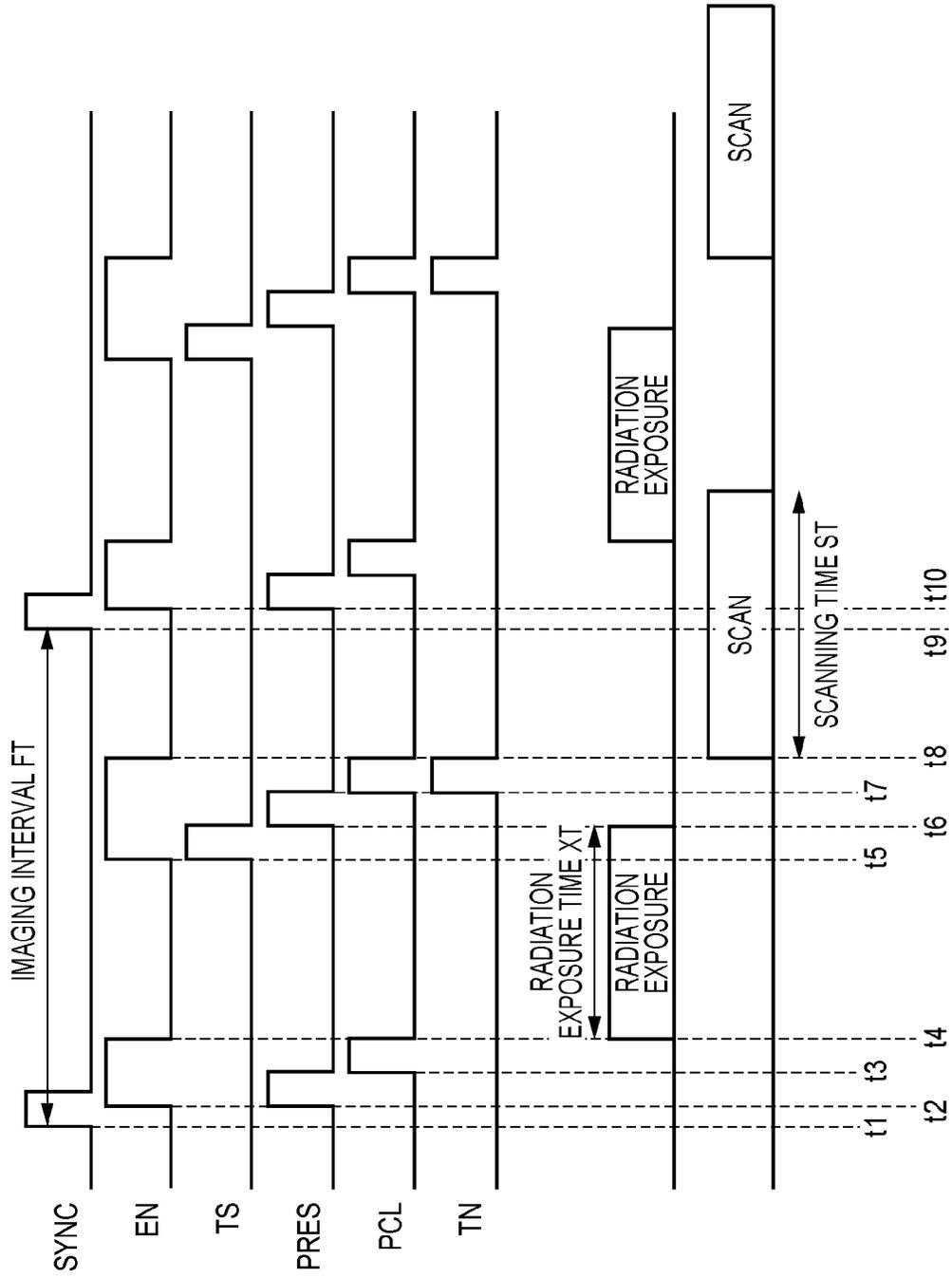


FIG. 5B



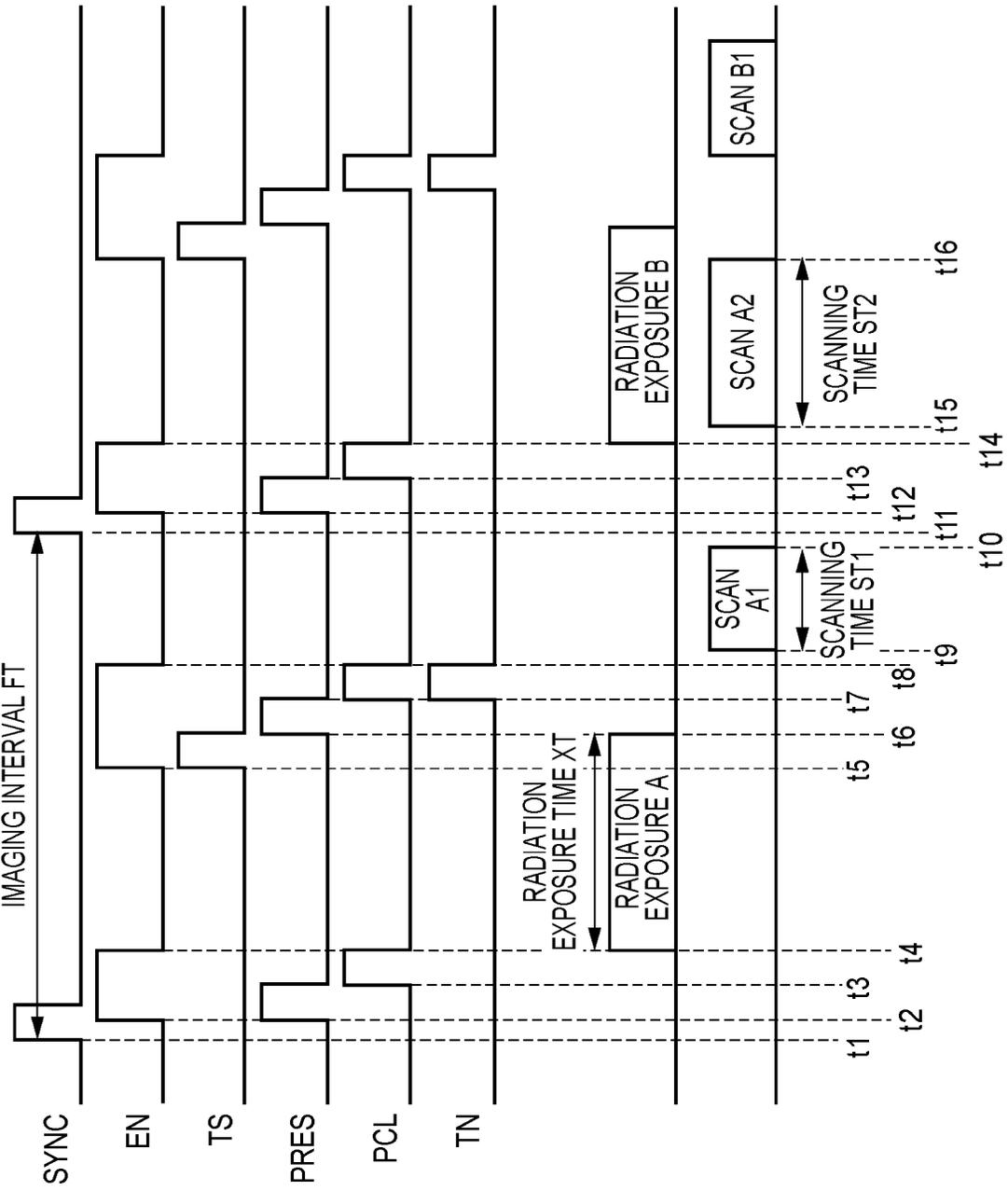
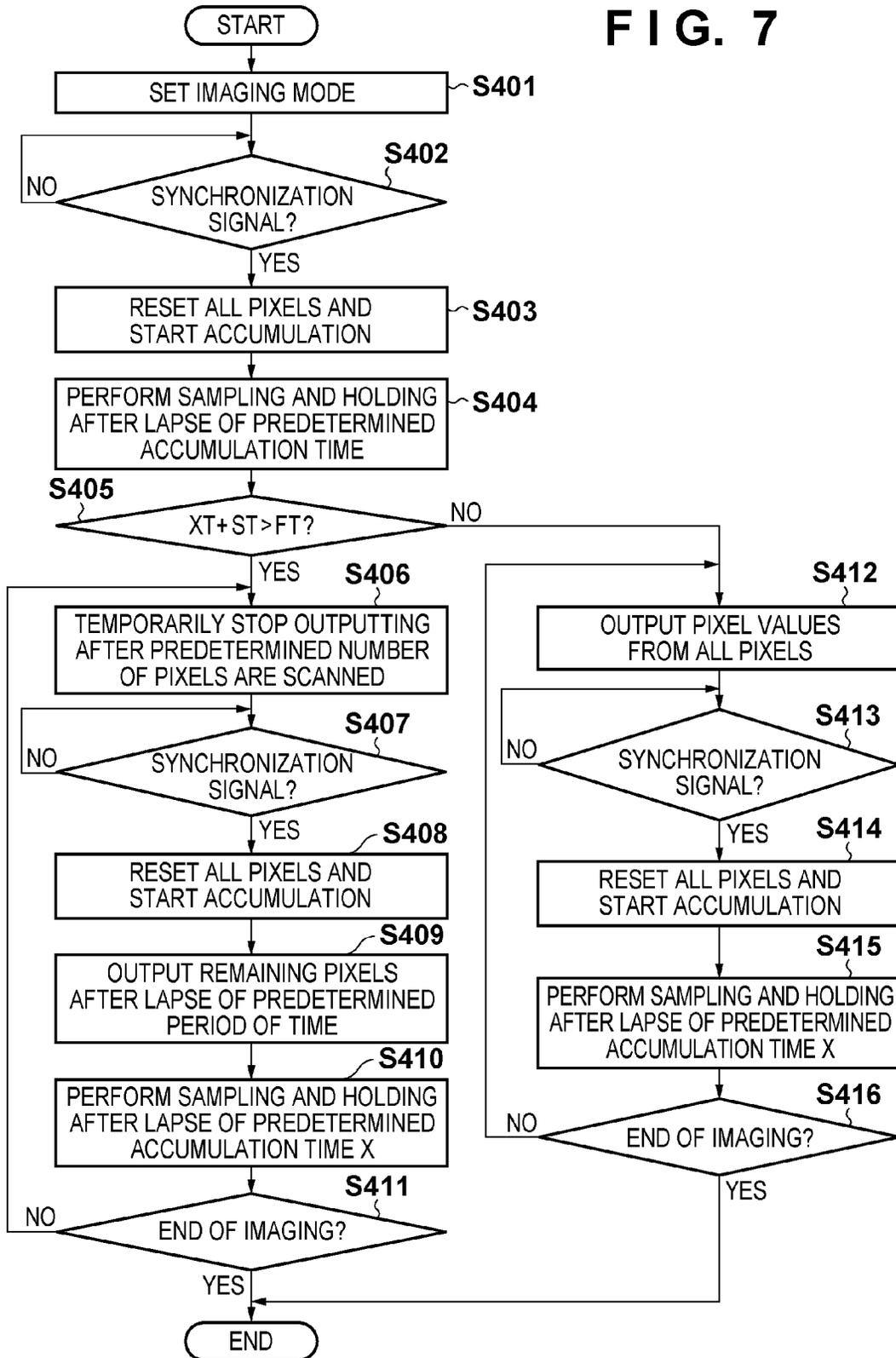


FIG. 6

FIG. 7



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**RADIATION IMAGING APPARATUS,  
CONTROL METHOD FOR RADIATION  
IMAGING APPARATUS, AND STORAGE  
MEDIUM**

CLAIM OF PRIORITY

This application claims the benefit of Japanese Patent Application No. 2010-230102 filed on Oct. 12, 2010, which is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a radiation imaging apparatus, a control method for the radiation imaging apparatus, a storage medium, and, more particularly, to a radiation imaging apparatus that reduces image artifacts upon imaging an object by intermittently irradiating the object with radiation in the form of pulses, a control method for the radiation imaging apparatus, and a storage medium.

2. Description of the Related Art

Recently, in the field of radiation imaging apparatuses, especially, digital X-ray imaging apparatuses, a large-area flat panel type radiation imaging apparatus based on a 1× optical system using photoelectric conversion elements has been widely used, instead of an image intensifier, for the purpose of increasing resolution, decreasing volume, and suppressing image distortion.

A large-area flat panel sensor formed by two-dimensionally joining photoelectric conversion elements generated on a silicon semiconductor wafer by a CMOS semiconductor manufacturing process is available as a flat panel sensor based on a 1× optical system that is used for a radiation imaging apparatus.

Japanese Patent Laid-Open No. 2002-026302 discloses a method of manufacturing a large-area flat panel sensor by tiling a plurality of rectangular semiconductor substrates that are rectangular imaging elements obtained by cutting photoelectric conversion elements in the form of strips from a silicon semiconductor wafer, in order to implement a large-area flat panel sensor equal to or larger than the silicon semiconductor wafer size.

In addition, Japanese Patent Laid-Open No. 2002-344809 discloses a circuit arrangement for each rectangular semiconductor substrate obtained by cutting out photoelectric conversion elements in the form of strips. On each of the rectangular semiconductor substrates cut out in the form of strips, vertical and horizontal shift registers as readout control circuits are arranged together with two-dimensionally arrayed photoelectric conversion elements. External terminals (electrode pads) are provided near the horizontal shift register. Control signals and clock signals input from the external terminals control the vertical and horizontal shift registers on each rectangular semiconductor substrate to cause the respective shift registers to sequentially output the respective pixel arrays in synchronism with the clock signals.

For example, as shown in FIG. 5A, no significant problem occurs when the sum of a scanning time ST required to output electrical signals from all of the photoelectric conversion elements and a radiation signal accumulation time XT (exposure time XT) is less than an imaging interval FT of a synchronization signal, that is, the frame rate is relatively low.

FIG. 5B shows an example of an imaging mode in which the sum of the scanning time ST required to output electrical signals from all of the photoelectric conversion elements and the radiation signal accumulation time XT (exposure time

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XT) is greater than the imaging interval FT of a synchronization signal. That is, this is an imaging mode in which the frame rate is relatively high, in which the shift registers on each rectangular semiconductor substrate are scanned to perform a resetting operation for starting accumulation of radiation signals at the time point indicated by t9 in FIG. 5B during an output period of an analog signal. If, however, a resetting operation is performed during an analog signal scan, currents simultaneously flow in all of the pixels on the rectangular semiconductor substrate to cause fluctuations in the power supply voltage of the rectangular semiconductor substrate. That is, an analog signal output during a resetting operation is disturbed to produce artifacts in a moving image.

The present invention provides a technique of obtaining a high-quality image by reducing artifacts even in a high-speed imaging mode, in consideration of the above problem.

SUMMARY OF THE INVENTION

According to one aspect, the present invention provides a radiation imaging apparatus comprising an output unit adapted to output an analog signal for each pixel circuit by sampling and holding an electrical signal converted from radiation, and a selection unit adapted to sequentially select positions of pixel circuits that output the analog signals, wherein after the output unit outputs the electrical signals corresponding to a predetermined number of pixel circuits as analog signals, the selection unit stops the selection and the output unit stops the output in accordance with the stoppage of the selection.

According to another aspect, the present invention provides a control method for a radiation imaging apparatus, comprising an output step of outputting an analog signal for each pixel circuit by sampling and holding an electrical signal converted from radiation, and a selection step of sequentially selecting positions of pixel circuits that output the analog signals, wherein after the electrical signals corresponding to a predetermined number of pixel circuits are output as analog signals in the output step, the selection is stopped in the selection step and the output is stopped in accordance with the stoppage of the selection in the selection step.

Further features of the present invention will be apparent from the following description of exemplary embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram showing an overall radiation moving image capturing system;

FIG. 2 is a view schematically showing the internal structure of a rectangular semiconductor substrate;

FIG. 3 is a timing chart showing an example of an image readout operation;

FIG. 4 is a circuit diagram showing an equivalent circuit corresponding to one pixel on a rectangular semiconductor substrate;

FIGS. 5A and 5B are timing charts of rectangular semiconductor substrate control signals;

FIG. 6 is a timing chart of rectangular semiconductor substrate control signals; and

FIG. 7 is a flowchart at the time of rectangular semiconductor substrate control.

DESCRIPTION OF THE EMBODIMENTS

An exemplary embodiment(s) of the present invention will now be described in detail with reference to the drawings. It

should be noted that the relative arrangement of the components, the numerical expressions, and numerical values set forth in these embodiments do not limit the scope of the present invention unless it is specifically stated otherwise.

#### First Embodiment

A schematic block diagram showing an overall radiation moving image capturing system based on a large-area flat panel system will be described with reference to FIG. 1. The radiation moving image capturing system includes a radiation imaging apparatus 100, an image processing/system control apparatus 101, an image display apparatus 102, an X-ray generator 103, and an X-ray tube 104. At the time of an imaging operation, the image processing/system control apparatus 101 synchronously controls the radiation imaging apparatus 100 and the X-ray generator 103. A scintillator (not shown) converts radiation transmitted through an object into visible light, which is subjected to photoelectric conversion in accordance with the amount of light. The resultant data is then A/D-converted. After A/D conversion, the radiation imaging apparatus 100 transfers the frame image data corresponding to the X-ray application to the image processing/system control apparatus 101. After image processing, the image display apparatus 102 displays the radiation image in real time.

The radiation imaging apparatus 100 includes a flat panel sensor 106. The flat panel sensor 106 includes rectangular semiconductor substrates 107 two-dimensionally cut out from a silicon semiconductor wafer in the form of strips. The rectangular semiconductor substrates 107 are tiled on a flat base (not shown) in a matrix of 14 columns $\times$ 2 rows. External terminals (electrode pads) (not shown) provided on the rectangular semiconductor substrates 107 arrayed in a matrix are arrayed in a line on each of the upper side portion and lower side portion of the flat panel sensor 106. The electrode pads provided on the rectangular semiconductor substrates 107 are connected to external circuits through flying lead type printed circuit boards (not shown). Analog multiplexers 131 to 138 select pixel outputs from the connected rectangular semiconductor substrates 107 in accordance with control signals from an imaging unit control circuit 108, and output the selected outputs to differential amplifiers 141 to 148, respectively connected to the analog multiplexers 131 to 138. A/D converters 151 to 158 convert analog signals from the differential amplifiers 141 to 148 into digital signals in accordance with synchronization clocks output from the imaging unit control circuit 108, and output the signals to the imaging unit control circuit 108. The imaging unit control circuit 108 combines digital image data having undergone A/D conversion in blocks by the A/D converters 151 to 158 into frame data, and transfers the frame data to the image processing/system control apparatus 101 via a connecting portion 109.

Each of the rectangular semiconductor substrates 107 cut out in the form of strips is a substrate having, for example, a width of about 20 mm and a length of about 140 mm. The flat panel sensor 106 formed by tiling the substrates in a matrix of 14 columns $\times$ 2 rows has, for example, a length of about 280 mm and a width of about 280 mm, that is, a square shape having a size of about 11 inches square.

The internal structure of the rectangular semiconductor substrate 107 will be described next with reference to FIG. 2. A timing chart showing an example of image readout processing from the flat panel sensor 106, on which the rectangular semiconductor substrates 107 are tiled, will be described with reference to FIG. 3.

Referring to FIG. 2, the rectangular semiconductor substrate 107 includes pixel circuits 201, a vertical shift register

202, and a horizontal shift register 203. A row control signal 204 is a signal in the row direction. A column control signal 205 is a signal in the column direction.

The pixel circuits 201 are pixel circuits including photoelectric conversion elements two-dimensionally arrayed on the rectangular semiconductor substrate 107. The vertical shift register 202 and the horizontal shift register 203 function as readout control circuits, which receive a horizontal shift register start signal HST, a vertical shift register start signal VST, a horizontal shift clock signal CLKH, and a vertical shift clock signal CLKV, via the external terminals.

Referring to the timing chart of FIG. 3, when the vertical shift clock signal CLKV rises while the vertical shift register start signal VST is at "H", the internal circuit of the vertical shift register 202 is reset. An "H" signal is then output to an output V0 of the vertical shift register 202 to enable pixel outputs corresponding to one line controlled by the row control signal 204. When the horizontal shift clock signal CLKH rises while the horizontal shift register start signal HST is at "H", the internal circuit of the horizontal shift register 203 is reset. An "H" signal is then output to an output H0 of the horizontal shift register 203 to output one of the pixel outputs enabled by the row control signal 204, which is output from the pixel circuit 201 selected by the output H0, to the analog output terminal. Horizontal shift clock signal CLKH pulses are sequentially input to the horizontal shift register 203 to sequentially shift the "H" output to H0, H1, . . . , H126, and H127, thus completing a readout operation corresponding to one line. The vertical shift clock signal CLKV is then input to the vertical shift register 202 to switch the "H" output to V1. Thereafter, pixel outputs corresponding to one line controlled by the row control signal 204 are enabled to perform a pixel readout operation. Sequentially repeating this operation will read out pixel outputs from the entire rectangular semiconductor substrate 107.

Since pixel values from the rectangular semiconductor substrate 107 are sequentially output to the external analog output terminal in synchronism with the horizontal shift clock signal CLKH, the A/D converter performs A/D conversion in response to an A/D conversion clock CLKAD synchronized with the horizontal shift clock signal CLKH.

FIG. 4 is a circuit diagram corresponding to one pixel on each tiled rectangular semiconductor substrate. Referring to FIG. 4, applying a reset voltage VRES to a switching MOS transistor 301 will reset a photodiode unit 302 and a floating diffusion capacitor 310. A switching MOS transistor 303 activates a MOS transistor 314 functioning as a floating diffusion amplifier. A switching MOS transistor 313 activates a MOS transistor 315 functioning as a source follower amplifier. A switching MOS transistor 304 is combined with a clamp capacitor 305 (capacitor 305) to form a clamp circuit, which can remove kTC noise (reset noise) generated by the photodiode unit 302. A switching MOS transistor 306 samples and holds a signal voltage corresponding to an amount of light. A switching MOS transistor 307 samples and holds the clamp voltage VCL. When the switching MOS transistor 306 is turned on, a capacitor 308 accumulates electrical charge. The capacitor 308 accumulates electrical charge corresponding to the voltage of the photodiode unit 302 to which noise and dark current components are added. When the switching MOS transistor 307 is turned on, a capacitor 309 accumulates electrical charge. The capacitor 309 accumulates electrical charge corresponding to the clamp voltage VCL, that is, noise and dark current components. Subtracting the electrical charge accumulated in the capacitor 309 from the electrical charge accumulated in the capacitor 308 can

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obtain a voltage corresponding to the amount of light from the photodiode unit **302**. The differential amplifiers **141** to **148** perform this subtraction.

The pixel value data obtained from the rectangular semiconductor substrate **107** contains the noise component generated by the photodiode unit **302**, which cannot be removed by subtracting the electrical charge accumulated in the capacitor **309** from the electrical charge accumulated in the capacitor **308**. For this reason, as is well known, such pixel value data is corrected by using pixel value data captured without application of radiation as fixed pattern noise (FPN), that is, an FPN image.

A sampling operation to be performed when a moving image is to be captured by intermittently irradiating an object with radiation in the form of pulses will be described with reference to FIGS. **4** and **5A**.

Referring to FIG. **5A**, at time **t1**, a synchronization signal SYNC is input from the image processing/system control apparatus **101**. When the synchronization signal SYNC is input, to start accumulation of radiation, the image processing/system control apparatus **101** sets the EN signal to High at time **t2** to turn on the switching MOS transistor **303** and the switching MOS transistor **313**. The image processing/system control apparatus **101** then activates the pixel circuit on the sensor chip and sets the PRES signal at High to turn on the switching MOS transistor **301**. The image processing/system control apparatus **101** applies the reset voltage VRES to the floating diffusion capacitor **310** to reset the sensor. The interval at which the synchronization signal SYNC is input corresponds to the imaging interval FT for a moving image.

At time **t3**, the image processing/system control apparatus **101** cancels the reset by turning off the switching MOS transistor **301** (PRES signal), and then sets the PCL signal at High to turn on the switching MOS transistor **304**, thereby applying the clamp voltage VCL to the clamp capacitor **305**.

At time **t4**, the image processing/system control apparatus **101** turns off the switching MOS transistor **303** (EN signal) and the switching MOS transistor **304** (PCL signal) to finish a pixel resetting operation and to start accumulation in the photodiode unit **302**, thus enabling the exposure of radiation.

The object is irradiated with radiation in the form of pulses for a predetermined period of time. Therefore, in order to minimize the influence of noise components generated by the photodiode unit **302**, the image processing/system control apparatus **101** finishes accumulation when a time corresponding to the application time of radiation has elapsed.

At time **t5**, the image processing/system control apparatus **101** sets the EN signal at High again to turn on the switching MOS transistor **303** and the switching MOS transistor **313** and to activate the pixel circuit on the sensor chip. The image processing/system control apparatus **101** then sets the TS signal at High to turn on the switching MOS transistor **306** and to cause the capacitor **308** to sample and to hold the voltage of the photodiode unit **302**.

At time **t6**, the image processing/system control apparatus **101** turns off the switching MOS transistor **306** (TS signal) to finish sampling and holding, and to disable the exposure of radiation. Subsequently, the image processing/system control apparatus **101** sets the PRES signal at High to turn on the switching MOS transistor **301** and to apply the reset voltage VRES to the floating diffusion capacitor **310**, thereby resetting the sensor.

At time **t7**, the image processing/system control apparatus **101** turns off the switching MOS transistor **301** (PRES signal), and then sets the PCL signal at High to turn on the switching MOS transistor **304** and to apply the clamp voltage VCL to the capacitor **305**. Subsequently, the image process-

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ing/system control apparatus **101** sets the TN signal at High to turn on the switching MOS transistor **307** and to cause the capacitor **309** to sample and to hold the clamp voltage VCL.

At time **t8**, the image processing/system control apparatus **101** finishes sampling and holding by turning off the switching MOS transistor **307** (TN signal), switching MOS transistor **304** (PCL signal), switching MOS transistor **303**, and switching MOS transistor **313** (EN signal). The image processing/system control apparatus **101** sequentially outputs the voltages sampled and held by the capacitor **308** and the capacitor **309** to the outside, by scanning the vertical and horizontal shift registers.

Although it is possible to change these driving timings according to predetermined settings, the set driving operation is repeated during an imaging operation to simplify control. That is, the image processing/system control apparatus **101** detects the synchronization signal SYNC again at time **t9**. Upon detecting the synchronization signal SYNC, the image processing/system control apparatus **101** sets the EN signal at High at time **t10** to turn on the switching MOS transistor **303** and the switching MOS transistor **313**, and to activate the pixel circuit on the sensor chip. The image processing/system control apparatus **101** repeats the above operation. The image processing/system control apparatus **101** simultaneously performs the above sampling operation for all pixels. This implements a collective electronic shutter operation and equalizes the accumulation times of the respective pixels, thereby preventing pixel value discontinuity caused by the tiling of the rectangular semiconductor substrates. The sampled and held voltages are read out as analog signals by scanning the shift registers in the horizontal and vertical directions for each rectangular semiconductor substrate. Converting this analog signal into a digital signal by the A/D converter will generate a digital image signal. Performing scanning while performing exposure of radiation can cope with a high frame rate at the time of moving image capturing, because it is possible to perform accumulation of radiation and scanning at the same timing.

A sampling operation to be performed when a moving image is captured by intermittently irradiating an object with radiation in the form of pulses will be described with reference to FIGS. **5A**, **5B**, **6**, and **7**.

First of all, in step **S401** in FIG. **7**, the radiation imaging apparatus **100** starts operation in the imaging mode set by the image processing/system control apparatus **101**. The imaging mode is, for example, imaging at a high or a low frame rate.

In step **S402**, the radiation imaging apparatus **100** determines whether a synchronization signal corresponding to the first image input from the image processing/system control apparatus **101** is detected. If the radiation imaging apparatus **100** determines that a synchronization signal is detected (YES in step **S402**), the process advances to step **S403**. If the radiation imaging apparatus **100** determines that no synchronization is detected (No in step **S402**), the process waits until a synchronization signal is detected.

In step **S403**, the image processing/system control apparatus **101** resets all of the pixels and starts accumulation of radiation. At time **t1** in FIG. **6**, when the first synchronization signal SYNC is input from the image processing/system control apparatus **101**, in order to start accumulation of radiation, the image processing/system control apparatus **101** sets the EN signal at High at time **t2** to turn on the switching MOS transistor **303** and the switching MOS transistor **313** to activate the pixel circuit on the sensor chip. At the same time, the image processing/system control apparatus **101** sets the PRES signal at High to turn on the switching MOS transistor **301** and to apply the reset voltage VRES to the photodiode

unit **302** and the floating diffusion capacitor **310**, thereby resetting the sensor. Subsequently, the image processing/system control apparatus **101** turns off the switching MOS transistor **301** (PRES signal) at time **t3** to cancel the reset. Thereafter, the image processing/system control apparatus **101** sets the PCL signal at High to turn on the switching MOS transistor **304** and to apply the clamp voltage VCL to the clamp capacitor **305** (capacitor **305**). At time **t4**, the image processing/system control apparatus **101** finishes a resetting operation by turning off the switching MOS transistor **304** (PCL signal) and the switching MOS transistor **301** (PRES signal). This starts accumulation in the photodiode unit **302** and enables exposure of radiation.

In step **S404**, after a predetermined accumulation time X elapses, the image processing/system control apparatus **101** performs sampling and holding. The object is irradiated with radiation in the form of pulses for a predetermined period of time. When the accumulation time X corresponding to the application time has elapsed, in order to finish accumulation, the image processing/system control apparatus **101** sets the EN signal at High at time **t5** to turn on the switching MOS transistor **303** and the switching MOS transistor **313** and activate the pixel circuit on the sensor chip. At the same time, the image processing/system control apparatus **101** sets the TS signal at High to turn on the switching MOS transistor **306** and to cause the capacitor **308** to sample and to hold the voltage of the photodiode unit **302**. When the image processing/system control apparatus **101** turns off the switching MOS transistor **306** (TS signal) at time **t6**, the sampling and holding operation ends, thus disabling the exposure of radiation. Subsequently, the image processing/system control apparatus **101** sets the PRES signal at High to turn on the switching MOS transistor **301** and to apply the reset voltage VRES to the floating diffusion capacitor **310**, thereby resetting the sensor. At time **t7**, the image processing/system control apparatus **101** turns off the switching MOS transistor **301** (PRES signal), and then sets the PCL signal at High to turn on the switching MOS transistor **304** and to apply the clamp voltage VCL to the capacitor **305**. The image processing/system control apparatus **101** then sets the TN signal at High to turn on the switching MOS transistor **307** and to cause the capacitor **309** to sample and to hold the clamp voltage VCL.

At time **t8**, the image processing/system control apparatus **101** turns off the switching MOS transistor **307** (TN signal), and turns off the switching MOS transistor **304** (PCL signal), the switching MOS transistor **303**, and the switching MOS transistor **313** (EN signal), thereby finishing a sampling and holding operation.

In step **S405**, the image processing/system control apparatus **101** decides the minimum imaging interval FT of a synchronization signal from the set imaging mode. The image processing/system control apparatus **101** determines whether the total time of the scanning time ST (also to be referred to as the output time ST) required to output electrical signals from all of the photoelectric conversion elements and the radiation signal accumulation time XT (also to be referred to as the exposure time XT) is greater than the imaging interval FT of the synchronization signal. If the image processing/system control apparatus **101** determines that the total time is longer than the imaging interval FT of the synchronization signal (YES in step **S405**), the process advances to step **S406**. If the image processing/system control apparatus **101** determines that the total time is shorter than the imaging interval FT of the synchronization signal (NO in step **S405**), the process advances to step **S412**. Since the timing of the driving signal in step **S412** is the same as that in FIG. **5A**, a description of this will be omitted.

Note that, in the above sampling operation, since currents simultaneously flow in all of the pixel circuits on the rectangular semiconductor substrate, the power supply voltage of the rectangular semiconductor substrate fluctuates.

In this embodiment, therefore, in step **S406**, the image processing/system control apparatus **101** waits for a predetermined period of time until fluctuations in power supply voltage converge. At time **t9** in FIG. **6**, the image processing/system control apparatus **101** scans each pixel circuit in which radiation is accumulated by radiation exposure A to start a scan **A1** to output the resultant value as an analog signal. When analog signals corresponding to a predetermined number of pixel circuits are output, the image processing/system control apparatus **101** temporarily stops scanning the shift registers at time **t10**. More specifically, the image processing/system control apparatus **101** stops inputting the horizontal shift register start signal HST, vertical shift register start signal VST, horizontal shift clock signal CLKH, and vertical shift clock signal CLKV to the vertical shift register **202** and the horizontal shift register **203**, in FIG. **2**, to temporarily stop outputting analog signals.

In step **S407**, the image processing/system control apparatus **101** determines at time **t11** in FIG. **6** whether the synchronization signal SYNC for the second image is detected. If the image processing/system control apparatus **101** determines that the synchronization signal SYNC is detected (YES in step **S407**), the process advances to step **S408**. If the image processing/system control apparatus **101** determines that the synchronization signal SYNC is not detected (NO in step **S407**), the process waits until the signal is detected.

In step **S408**, in order to start accumulation of radiation, the image processing/system control apparatus **101** sets the EN signal at High at time **t12** to turn on the switching MOS transistor **303** and the switching MOS transistor **313**, and to activate the pixel circuit on the sensor chip. At the same time, the image processing/system control apparatus **101** sets the PRES signal at High to turn on the switching MOS transistor **301** and to apply the reset voltage VRES to the photodiode unit **302** and the floating diffusion capacitor **310**, thereby resetting the sensor.

At this time, since currents flow in all of the pixel circuits, the power supply voltage of the semiconductor circuit substrate fluctuates. However, since scanning is temporarily stopped, output analog signals are not disturbed. Depending on the arrangement of a pixel circuit, however, fluctuations in power supply voltage may give offsets to sampled and held analog signals. The offsets generated by the fluctuations in power supply voltage are constant. It is, therefore, possible to acquire an FPN image (fixed pattern noise image) for offset correction of a noise portion upon the same driving operation as that described above, before the radiation exposure, and to cancel an offset based on the difference between a radiation image and the pixel value data of the FPN image for offset correction.

Subsequently, at time **t13**, the image processing/system control apparatus **101** cancels the reset by turning off the switching MOS transistor **301** (PRES signal). The image processing/system control apparatus **101** then sets the PCL signal at High to turn on the switching MOS transistor **304**, and to apply the clamp voltage VCL to the capacitor **305**. At time **t14**, the image processing/system control apparatus **101** finishes the resetting operation of the pixel by turning off the switching MOS transistor **304** (PCL signal), the switching MOS transistor **303**, and the switching MOS transistor **313** (EN signal). This causes the photodiode unit **302** to start accumulation, and enables radiation exposure B.

The power supply voltage of the semiconductor circuit board fluctuates due to a resetting operation, from time t12 to time t14. After a predetermined period of time elapses until the fluctuations in power supply voltage converge, the image processing/system control apparatus 101 resumes a scan A2 at time t15 to cause the semiconductor circuit board to output an analog signal that has not been output (S409 to S411). At time t16, the image processing/system control apparatus 101 stops scanning when all of the semiconductor circuit boards output analog signals. At this time, the image processing/system control apparatus 101 decides a scanning time ST1, such that a scanning time ST2 for the scan A2 becomes equal to or less than the exposure time XT. The number of pixels to be scanned in the scan A1 may be the number of pixels corresponding to the scanning time ST1.

For example, as shown in FIG. 1, the number of pixels on the rectangular semiconductor substrate 107 is  $128 \times 896 = 114688$ , and the horizontal shift clock signal CLKH has a frequency of 20 MHz. The scanning time ST corresponds to the time required to scan the four rectangular semiconductor substrates 107, and hence

$$ST = 114688 \times (\frac{1}{20M}) \times 4 = \text{about } 23 \text{ ms.}$$

If the frame rate is 15 FPS, the imaging interval FT is given by:

$$FT = \frac{1}{15} = 66.7 \text{ ms.}$$

If the accumulation time XT (exposure time XT) of a radiation signal is 16 ms, then

$$XT + ST = 16 \text{ ms} + 23 \text{ ms} = 39 \text{ ms} < FT = 66.7 \text{ ms.}$$

In this case, therefore, the process shifts from step S405 to step S412 in FIG. 7, and shift register scanning is controlled in the manner shown in FIG. 5A without a temporary stop (S412 to S416).

However, if the frame rate is further increased to 30 FPS, the imaging interval FT is given by:

$$FT = \frac{1}{30} = 33.3 \text{ ms.}$$

If, therefore, the accumulation time XT of a radiation signal is 16 ms, then

$$XT + ST = 16 \text{ ms} + 23 \text{ ms} = 39 \text{ ms} > FT = 33.3 \text{ ms.}$$

The process shifts from step S405 to step S406 in FIG. 7. The image processing/system control apparatus 101 temporarily stops scanning the shift registers, and performs a control operation in the manner as shown in FIG. 6. At this time, if scanning time ST2=14 ms < XT=16 ms, in consideration of the reset time, for example, the scanning time ST1 may be set to 9 ms. When scanning the number of pixels corresponding to 9 ms, the image processing/system control apparatus 101 temporarily stops scanning.

As described above, when a predetermined number of pixels are scanned, scanning is temporarily stopped until the detection of a synchronization signal. With this operation, even if jitter occurs in a synchronization signal, the number of pixels to be scanned remains the same before and after a resetting operation. For this reason, it is also possible to reduce artifacts by acquiring an FPN image for offset correction and calculating the difference between the FPN image and a radiation image. This makes it possible to output a high-quality radiation image.

#### Second Embodiment

In the first embodiment, when the number of pixels scanned has reached a predetermined number, the image processing/system control apparatus 101 temporarily disables

the horizontal shift register start signal HST, vertical shift register start signal VST, horizontal shift clock signal CLKH, and vertical shift clock signal CLKV input to the vertical shift register 202, and the horizontal shift register 203, and detects a synchronization signal. However, the present invention is not limited to this method. The apparatus may be configured to temporarily disable a horizontal shift register start signal HST, vertical shift register start signal VST, horizontal shift clock signal CLKH, and vertical shift clock signal CLKV, upon scanning a predetermined number of rows, and to detect a synchronization signal.

This makes it possible to control the temporary stoppage and resumption of shift register scanning by only counting the vertical shift clock signal CLKV. This can facilitate control of the shift registers. In addition, since the apparatus temporarily stops and resumes shift register scanning for each line, artifacts are made less noticeable.

In addition, it is possible to control shift register scanning for each control signal from analog multiplexers 131 to 138, which are used to select an analog output from a plurality of rectangular semiconductor substrates 107. This can improve the setting accuracy of scanning times ST1 and ST2.

According to the present invention, it is an object to obtain a high-quality image by reducing artifacts in the high-speed imaging mode.

#### Other Embodiments

Aspects of the present invention can also be realized by a computer of a system or an apparatus (or devices such as a CPU or an MPU) that reads out and executes a program recorded on a memory device to perform the functions of the above-described embodiment(s), and by a method, the steps of which are performed by a computer of a system or an apparatus by, for example, reading out and executing a program recorded on a memory device to perform the functions of the above-described embodiment(s). For this purpose, the program is provided to the computer, for example, via a network or from a recording medium of various types serving as the memory device (for example, a computer-readable storage medium).

While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

What is claimed is:

1. A radiation imaging apparatus comprising:
  - an accumulation unit adapted to accumulate electrical charge in accordance with exposure to generated radiation in each pixel circuit of a plurality of pixel circuits;
  - an output unit adapted to output an analog signal for each pixel circuit by sampling and holding an electrical signal in accordance with a voltage of an accumulation unit for each pixel circuit, wherein the output unit stops the output during a reset operation of the accumulation unit;
  - a selection unit adapted to select pixel circuits that output the analog signals, wherein the selection unit stops the selection during a reset operation of the accumulation unit;
  - a detection unit adapted to detect a synchronization signal representing a radiation generation timing; and
  - a determination unit adapted to determine whether a total time of an exposure time and an output time required to output the analog signals corresponding to all of the

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pixel circuits is longer than an imaging interval that is based on the synchronization signal,  
 wherein, when the determination unit determines that the total time is longer than the imaging interval, the selection unit stops the selection and the output unit stops the output, in accordance with the stoppage of the selection, after the output unit outputs the electrical signals corresponding to a predetermined number of pixel circuits as analog signals.

2. The apparatus according to claim 1, further comprising a control unit adapted to control the output unit to sample and to hold the electrical signal after starting of the radiation generated, for exposure, at the imaging interval corresponding to the synchronization signal, and the exposure time elapses,

wherein the radiation is irradiated to the accumulation unit in the form of pulses having the exposure time that is shorter than the imaging interval, and

wherein the selection unit starts a sequential selection of the pixel circuits between the reset operation of the accumulation unit.

3. The apparatus according to claim 2, wherein a photodiode and a capacitor of each of the pixel circuits are reset when the detection unit detects the synchronization signal again, the selection unit resumes the selection, and the output unit resumes the output at a position of a remaining pixel circuit, after a predetermined period of time elapses since a start of exposure of the radiation at the imaging interval corresponding to the synchronization signal, before the exposure time elapses.

4. The apparatus according to claim 3, further comprising a correction unit adapted to correct a noise offset based on a difference between a radiation image, based on the analog signal output from the output unit and pixel value data of fixed pattern noise acquired by the output unit in advance, based on the analog signal output in advance, before the exposure of the radiation.

5. The apparatus according to claim 4, wherein the selection unit selects a position of a pixel circuit, for each array of pixel circuits, which outputs the analog signal.

6. A control method for a radiation imaging apparatus, the control method comprising:

an accumulation step of accumulating electrical charge into an accumulation unit in accordance with exposure to generated radiation in each pixel circuit of a plurality of pixel circuits;

an output step of outputting an analog signal for each pixel circuit by sampling and holding an electrical signal in accordance with a voltage of an accumulation unit for each pixel circuit, wherein, in the output step, the output is stopped during a reset operation of the accumulation unit;

a selection step of selecting pixel circuits that output the analog signals, wherein, in the selection step, the selection is stopped during a reset operation of the accumulation unit;

a detection step of detecting a synchronization signal representing a radiation generation timing; and

a determination step of determining whether a total time of an exposure time and an output time required to output the analog signals corresponding to all of the pixel circuits is longer than an imaging interval that is based on the synchronization signal, wherein, when the determination step determines that the total time is longer than the imaging interval, the selection is stopped in the selection step and the output is stopped in the output step, in accordance with the stoppage of the selection,

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after electrical signals are outputted in the output step corresponding to a predetermined number of pixel circuits.

7. A radiation imaging apparatus comprising:

a plurality of pixel circuits, each of the plurality of pixel circuits comprising (i) a conversion unit adapted to convert generated radiation to a signal, (ii) a sampling and holding unit adapted to sample and to hold the signal, (iii) an output unit adapted to output the signal sampled and held by the sampling and holding unit, and (iv) a resetting unit adapted to reset the conversion unit;

a selection unit adapted to perform a selection operation of a pixel circuit that is to output the sampled and held signal, in order to output the sampled and held signal from the plurality of pixel circuits;

a control unit adapted to control the plurality of pixel circuits so that the reset is collectively performed to the plurality of pixel circuits, based on a signal indicative of radiation generation timing that is detected by the control unit, and the sampling and holding is collectively performed to the plurality of pixel circuits; and

a determination unit adapted to determine whether or not the selection operation to the plurality of pixel circuits, based on an immediately preceding signal indicative of the timing is completed, when the reset is performed based on the signal indicative of the timing,

wherein, if the determination unit determines that the selection operation is not completed, the selection unit stops the selection operation in which a portion of pixel circuits, out of the plurality of pixel circuits, remains unselected, and resumes the selection operation to the portion of the pixel circuits after the control unit performs the reset.

8. The apparatus according to claim 7, wherein the radiation is irradiated to the plurality of pixel circuits in the form of pulses having an exposure time that is shorter than an imaging interval defined by an interval of two consecutive signals representing the timing,

wherein the selection unit starts a selection operation of the pixel circuits between the reset operation of the resetting unit, and

wherein the selection unit performs the selection operation to the portion of the pixel circuits after a predetermined time elapses from the reset having been performed by the control unit.

9. The apparatus according to claim 7, wherein the selection unit performs the selection operation after a predetermined time elapses from the reset having been performed by the control unit.

10. The apparatus according to claim 7, further comprising a correction unit adapted to obtain pixel value data of fixed-pattern noise based on a signal preliminarily outputted by the output unit before a radiation exposure, and to correct an offset of noise based on the difference between the obtained pixel value data and a radiation image that is based on a signal outputted by the output unit.

11. A computer-readable non-transitory storage medium storing a program for causing a computer to execute each step in a control method for a radiation imaging apparatus, the control method comprising:

an accumulation step of accumulating electrical charge into an accumulation unit in accordance with exposure to generated radiation in each pixel circuit of a plurality of pixel circuits;

an output step of outputting an analog signal for each pixel circuit by sampling and holding an electrical signal in accordance with a voltage of an accumulation unit for

each pixel circuit, wherein, in the output step, the output is stopped during a reset operation of the accumulation unit;

a selection step of selecting pixel circuits that output the analog signals, wherein, in the selection step, the selection is stopped during a reset operation of the accumulation unit;

a detection step of detecting a synchronization signal representing a radiation generation timing; and

a determination step of determining whether a total time of an exposure time and an output time required to output analog signals corresponding to all of the pixel circuits is longer than an imaging interval that is based on the synchronization signal, wherein, when the determination step determines that the total time is longer than the imaging interval, the selection is stopped in the selection step and the output is stopped in the output step, in accordance with the stoppage of the selection, after electrical signals are outputted in the output step corresponding to a predetermined number of pixel circuits.

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