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(54) **BUILT-IN REDUNDANCY SCHEME FOR COMMUNICATION SYSTEM ON CHIP**

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(51) **Int. Cl.**

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H04B 10/40	(2013.01)
H04B 10/556	(2013.01)
H04B 10/54	(2013.01)
H04B 10/516	(2013.01)
H04B 10/69	(2013.01)
H04J 14/02	(2006.01)

(52) **U.S. Cl.**
CPC ***H04B 10/801*** (2013.01); ***H04B 10/40*** (2013.01); ***H04B 10/5161*** (2013.01); ***H04B 10/541*** (2013.01); ***H04B 10/5561*** (2013.01); ***H04B 10/69*** (2013.01); ***H04J 14/02*** (2013.01)

(58) **Field of Classification Search**
CPC H04B 10/40; H04B 10/501–10/503; H04B 10/508–10/588
See application file for complete search history.

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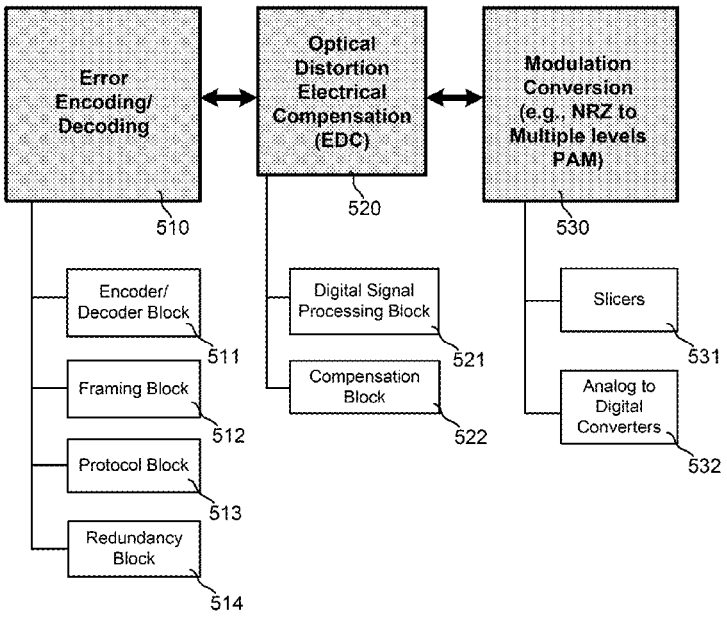
(57) **ABSTRACT**

In an example, the present invention includes an integrated system on chip device. The device has a redundancy block is configured to add at least redundancy bit as a function of one or more data bits associated with data for data error detection and correction data. In an example, the driver module is coupled to the signal processing blocking using a uni-directional multi-lane bus configured with N lanes, whereupon N is greater than M such that a difference between N and M represents a redundant lane or lanes. The device also has a mapping block configured to associate the M lanes to a plurality of selected laser devices for a silicon photonics device.

18 Claims, 13 Drawing Sheets



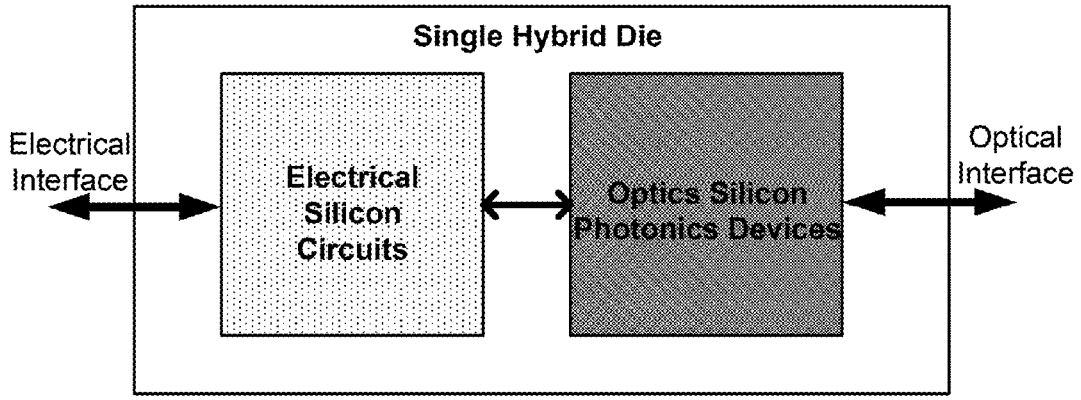

Single Hybrid Die
Electrical Interface
Electrical Silicon Circuits
Optics Silicon Photonics Devices
Optical Interface

Fig. 1

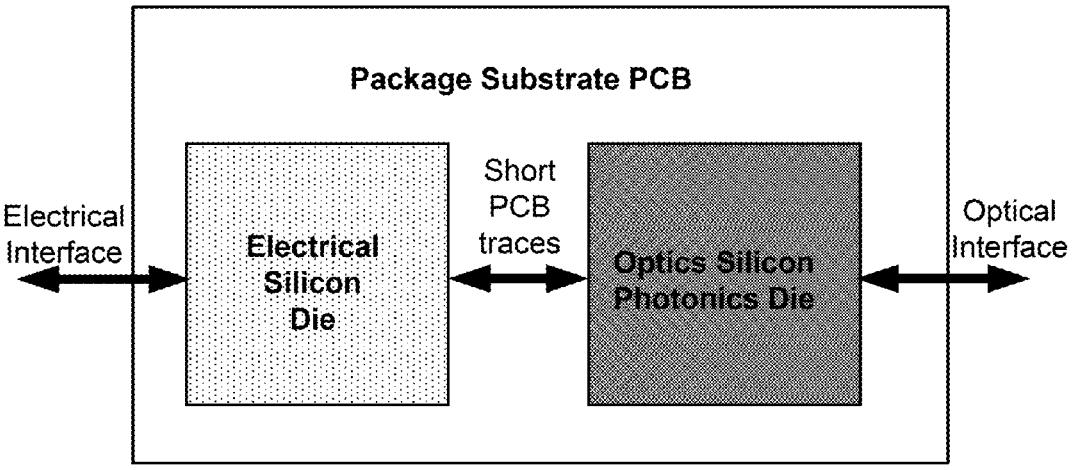

Package Substrate PCB
Electrical Interface
Electrical Silicon Die
Short PCB traces
Optics Silicon Photonics Die
Optical Interface

Fig. 2

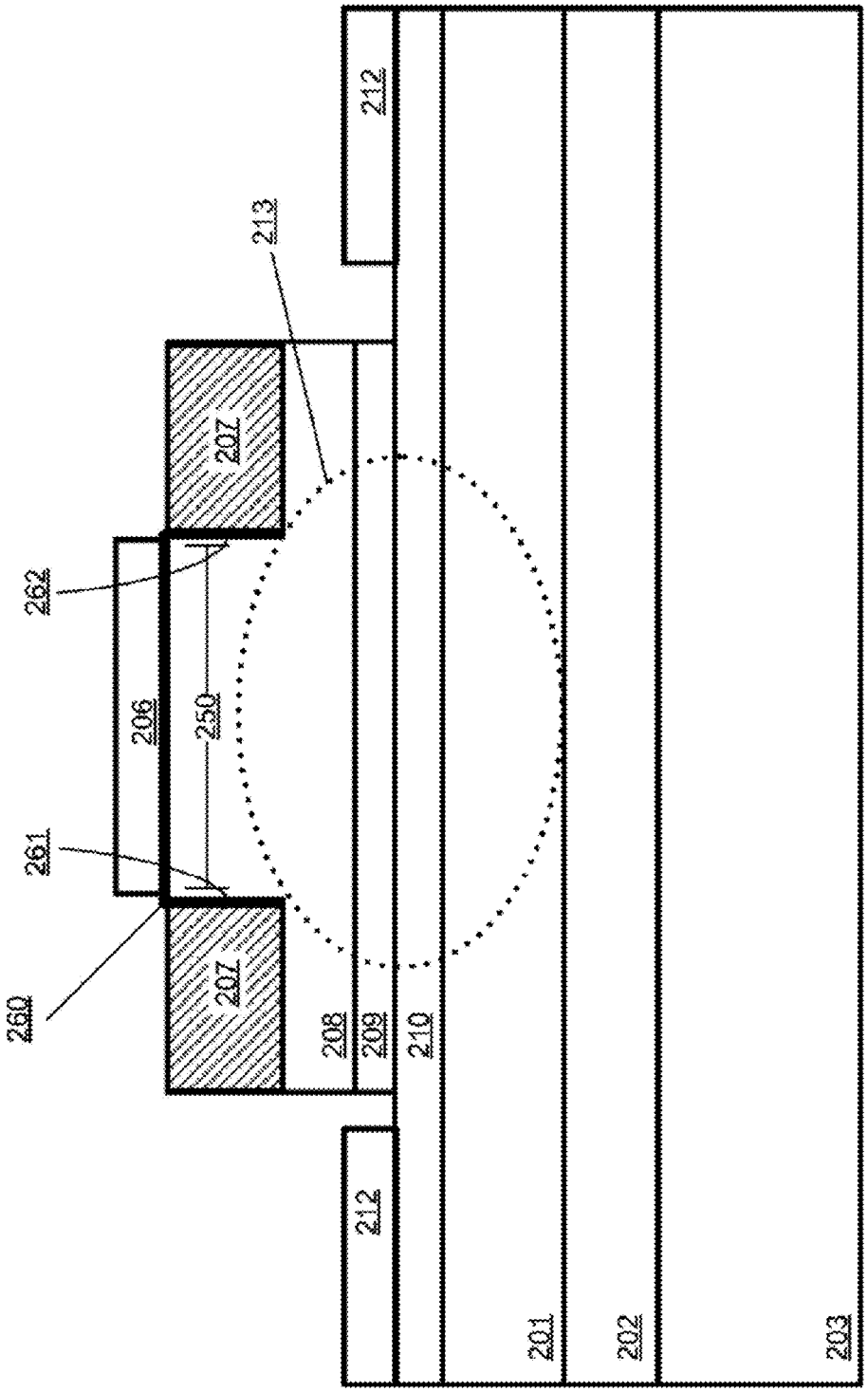

212
213
207
262
206
250
261
260
207
208
209
210
212
201
202
203
200

Fig. 2A

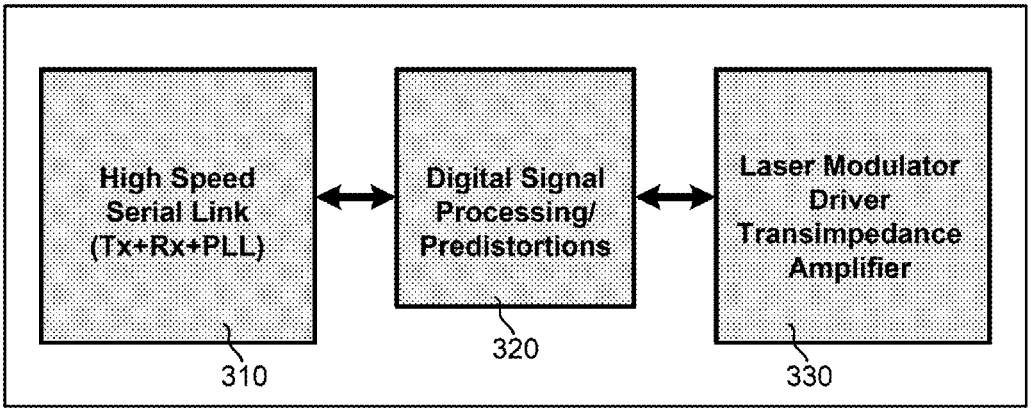

High Speed Serial Link (Tx+Rx+PLL)
Digital Signal Processing/ Predistortions
Laser Modulator Driver Transimpedance Amplifier
310
320
330

Fig. 3

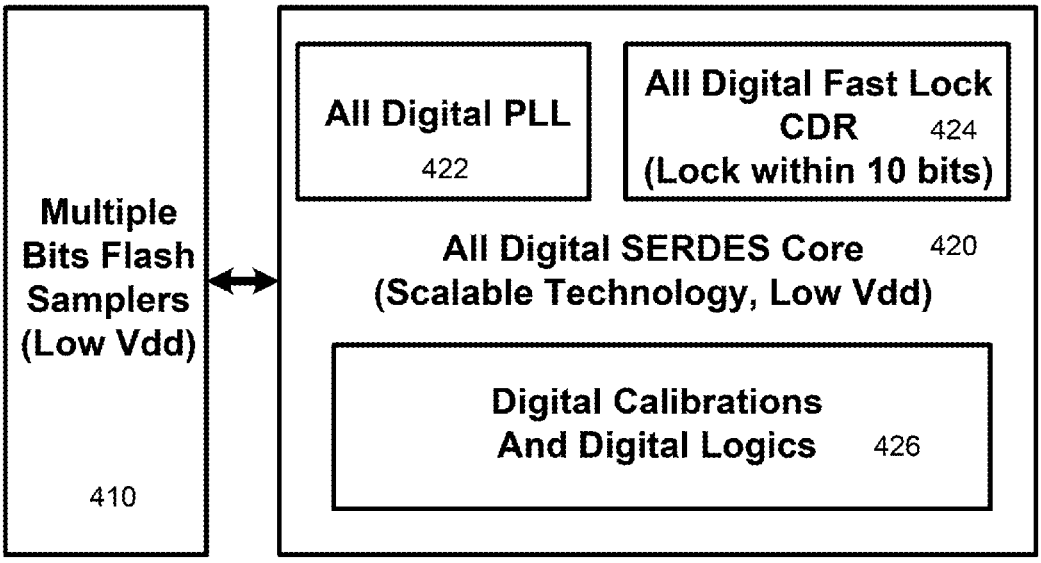

Multiple Bits Flash Samplers (Low Vdd)
410
All Digital PLL
422
All Digital Fast Lock CDR
424
(Lock within 10 bits)
All Digital SERDES Core
420
(Scalable Technology, Low Vdd)
Digital Calibrations And Digital Logics
426

Fig. 4

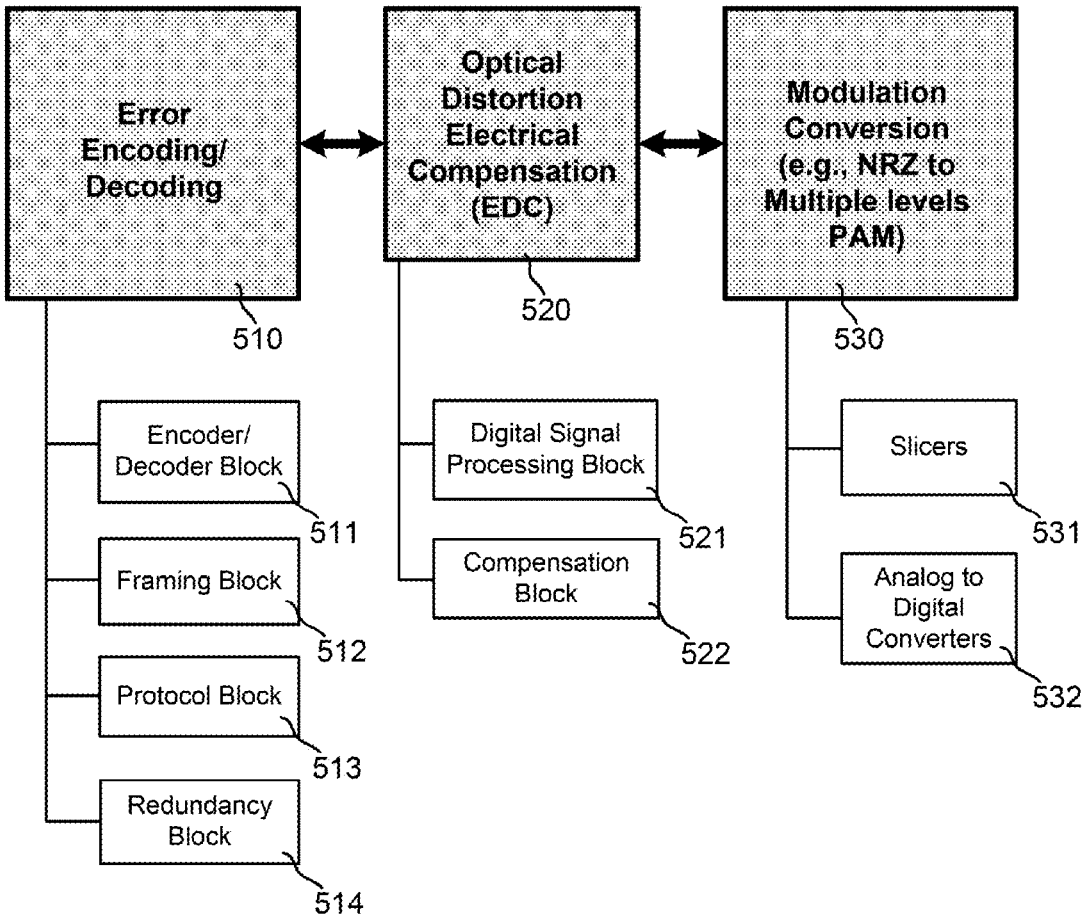

Error Encoding/ Decoding
510
Optical Distortion Electrical Compensation (EDC)
520
Modulation Conversion (e.g., NRZ to Multiple levels PAM)
530
Encoder/ Decoder Block
511
Framing Block
512
Protocol Block
513
Redundancy Block
514
Digital Signal Processing Block
521
Compensation Block
522
Slicers
531
Analog to Digital Converters
532

Fig. 5

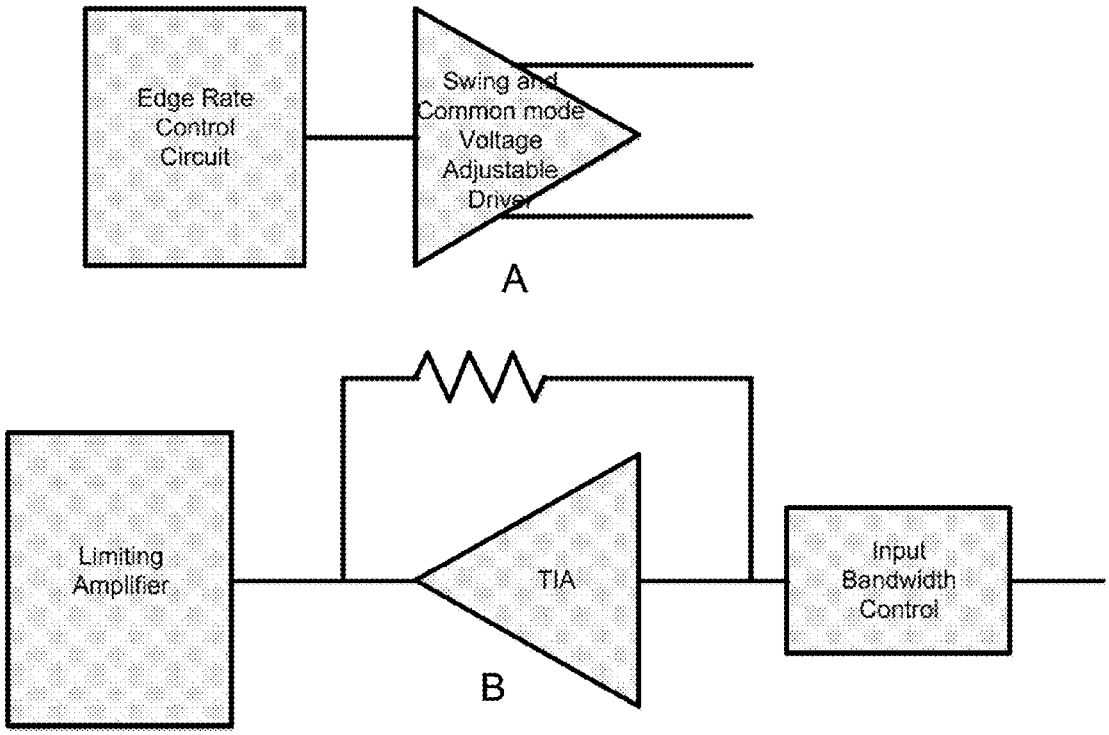

Edge Rate Control Circuit
Swing and Common mode Voltage Adjustable Driver
A
Limiting Amplifier
TIA
Input Bandwidth Control
B

Fig. 6

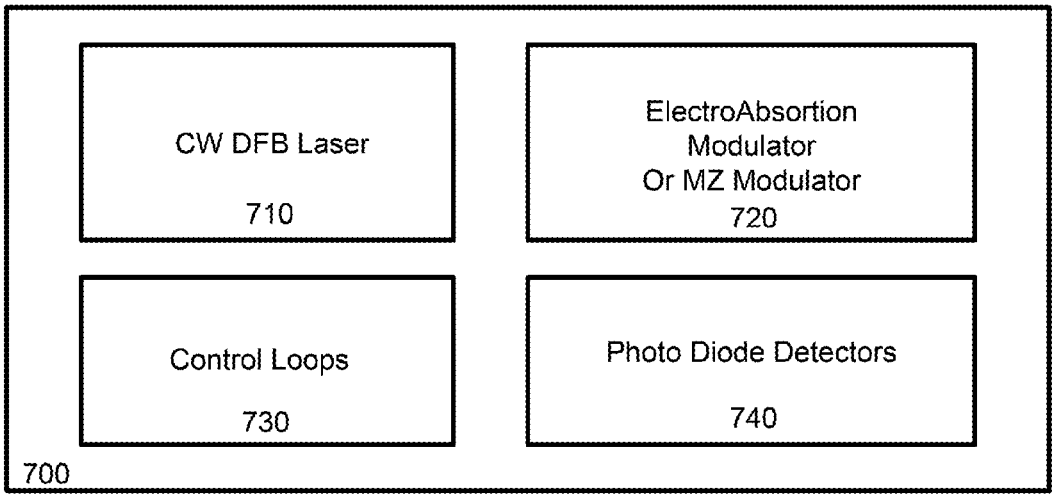

CW DFB Laser
710
ElectroAbsortion
Modulator
Or MZ Modulator
720
Control Loops
730
Photo Diode Detectors
740
700

Fig. 7

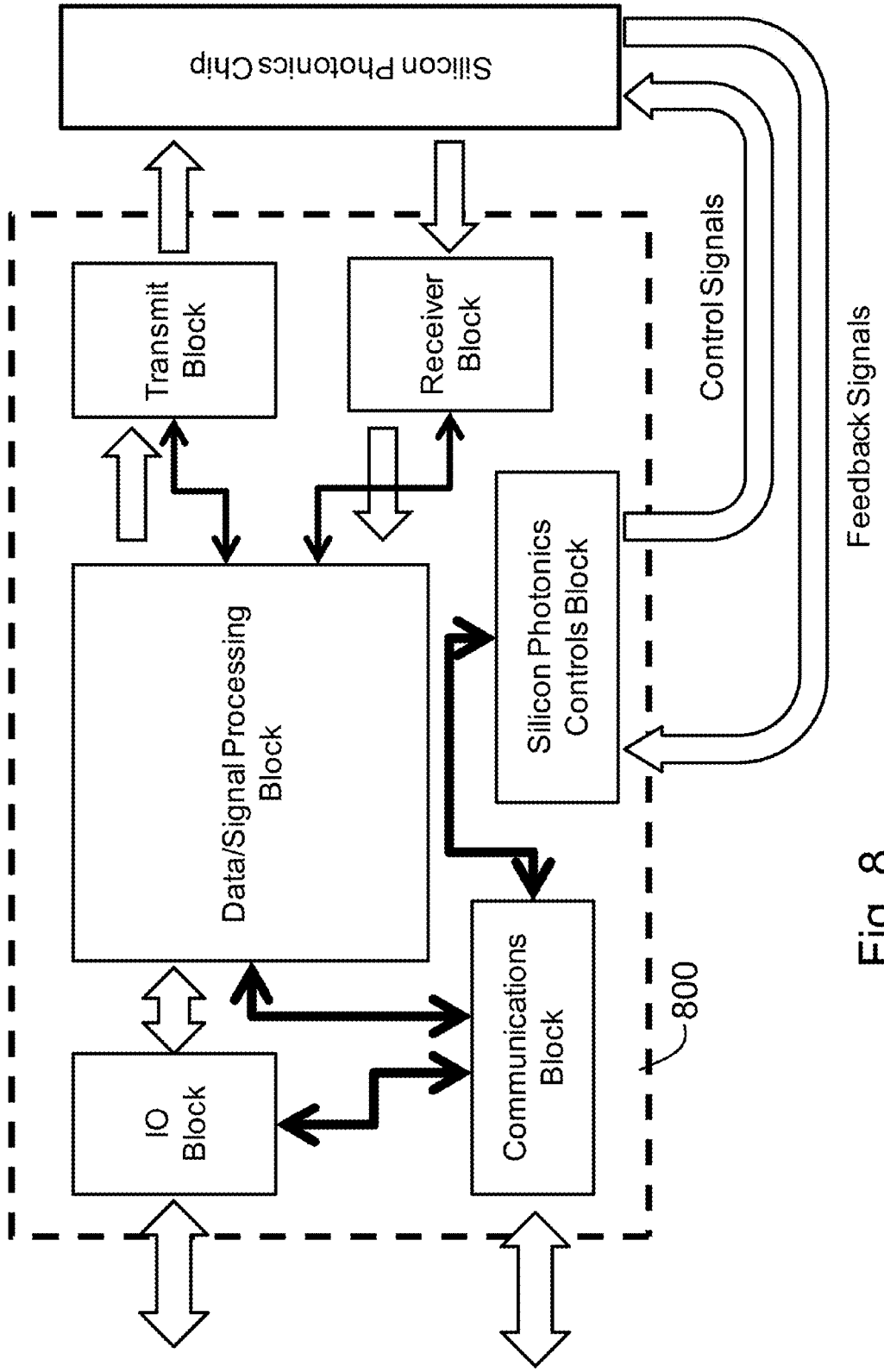

Silicon Photonics Chip
Transmit Block
Receiver Block
Control Signals
Feedback Signals
Silicon Photonics Controls Block
Data/Signal Processing Block
Communications Block
IO Block
800

Fig. 8

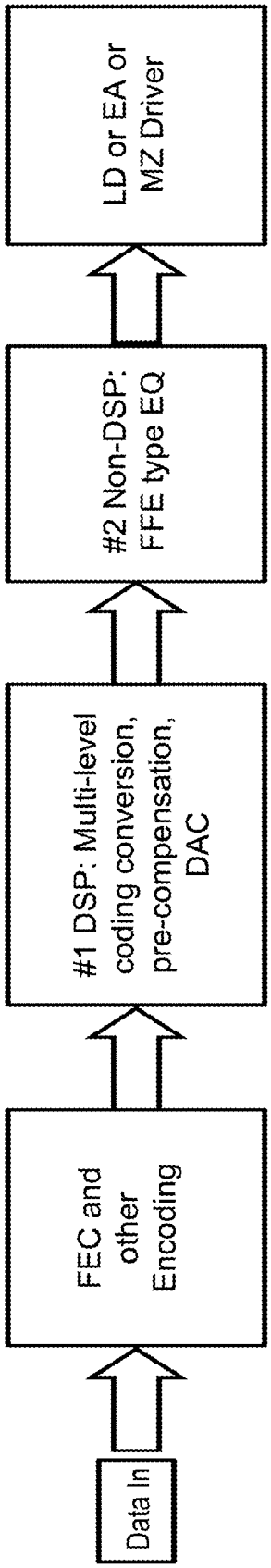

Data In
FEC and other Encoding
#1 DSP: Multi-level coding conversion, pre-compensation, DAC
#2 Non-DSP: FFE type EQ
LD or EA or MZ Driver

Fig. 9

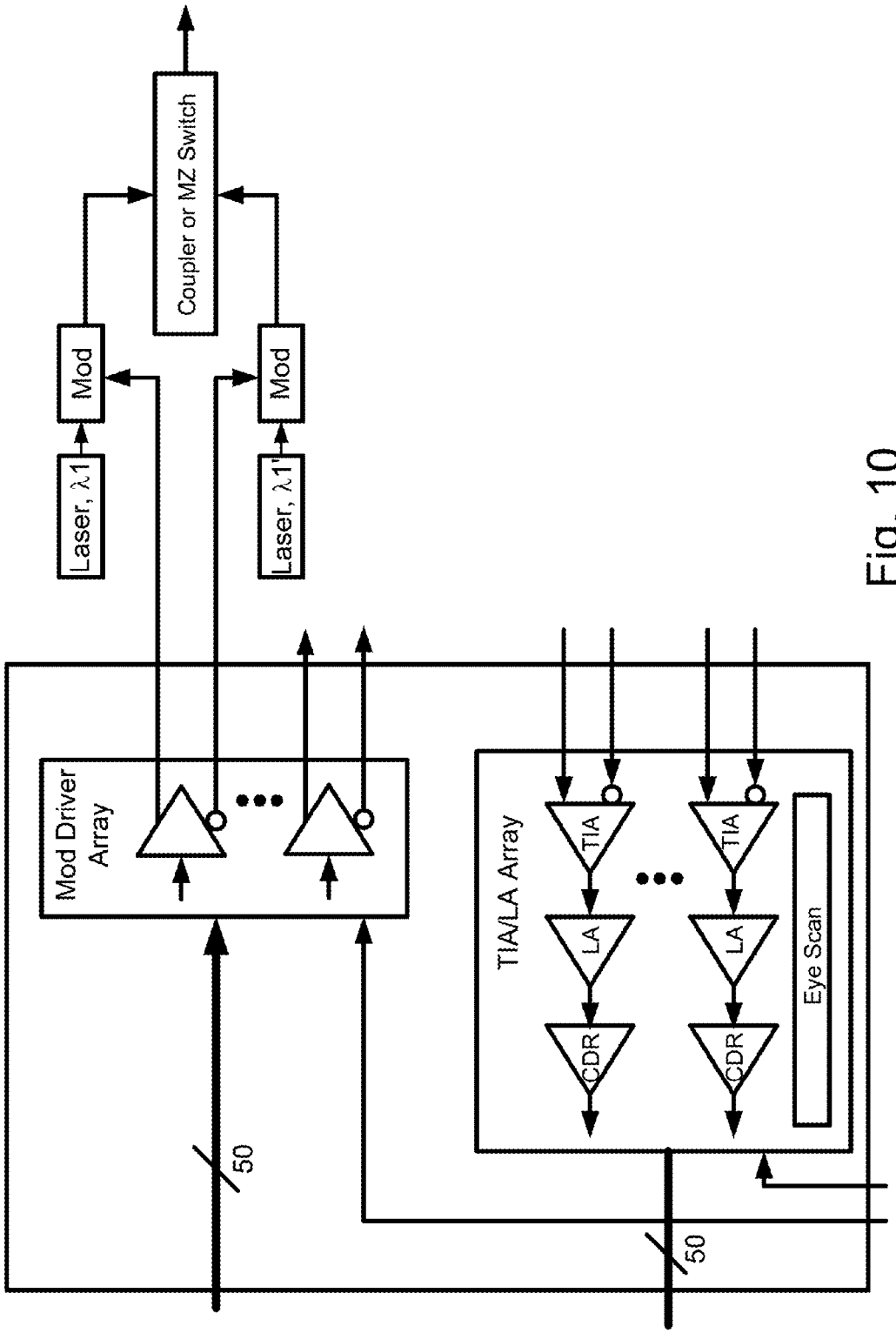

Coupler or MZ Switch
Mod
Mod
Laser, λ1
Laser, λ1'
Mod Driver Array
TIA/LA Array
TIA
TIA
LA
LA
CDR
CDR
Eye Scan
50
50

Fig. 10

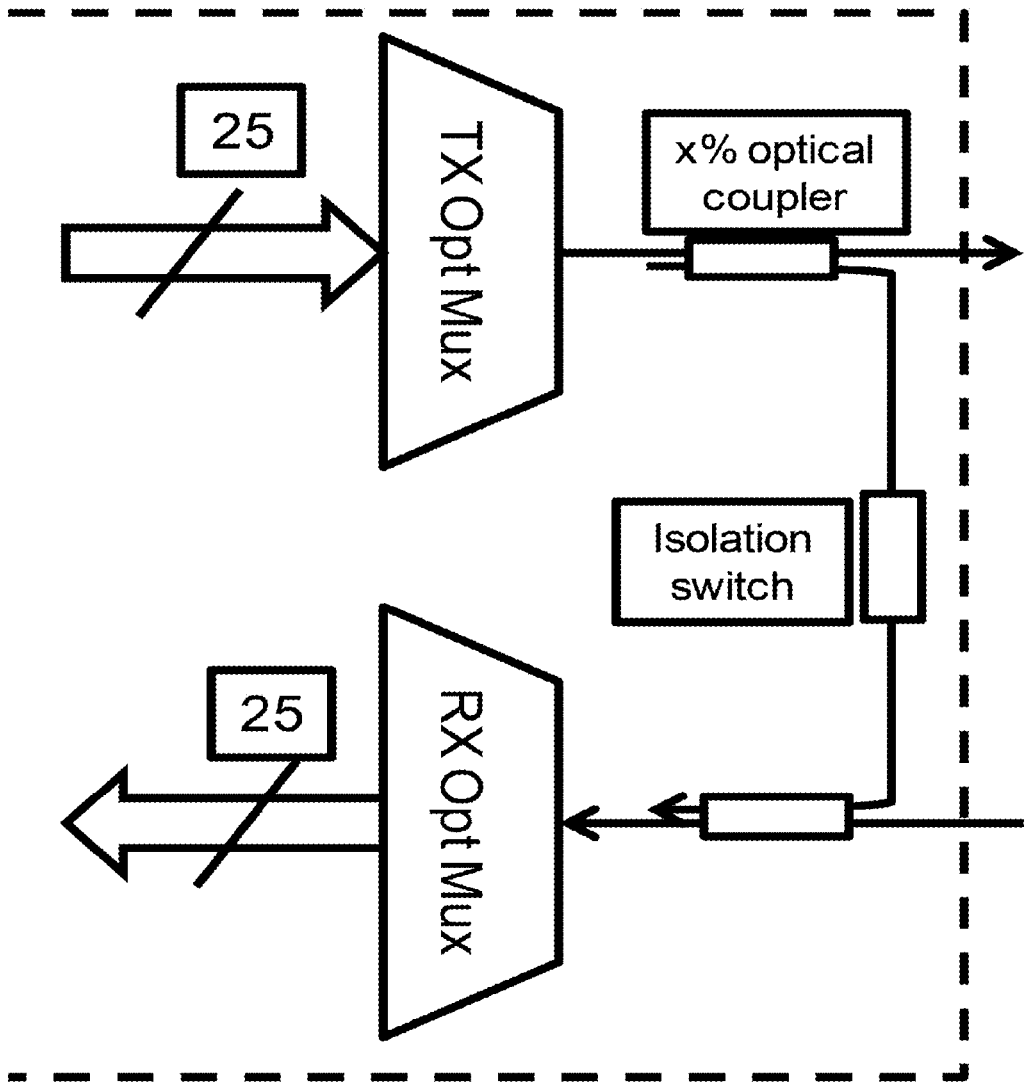

25
TX Opt Mux
x% optical coupler
Isolation switch
25
RX Opt Mux

Fig. 11

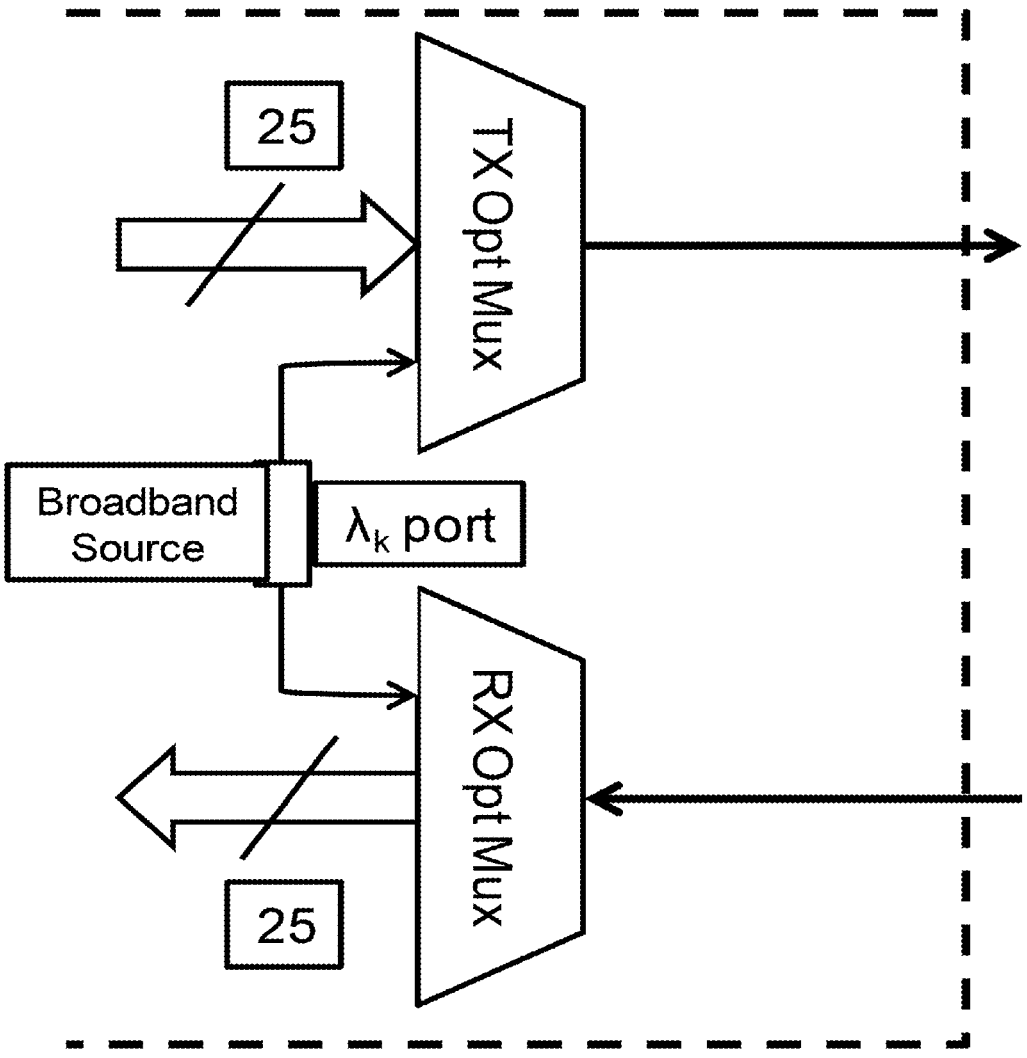


Fig. 12

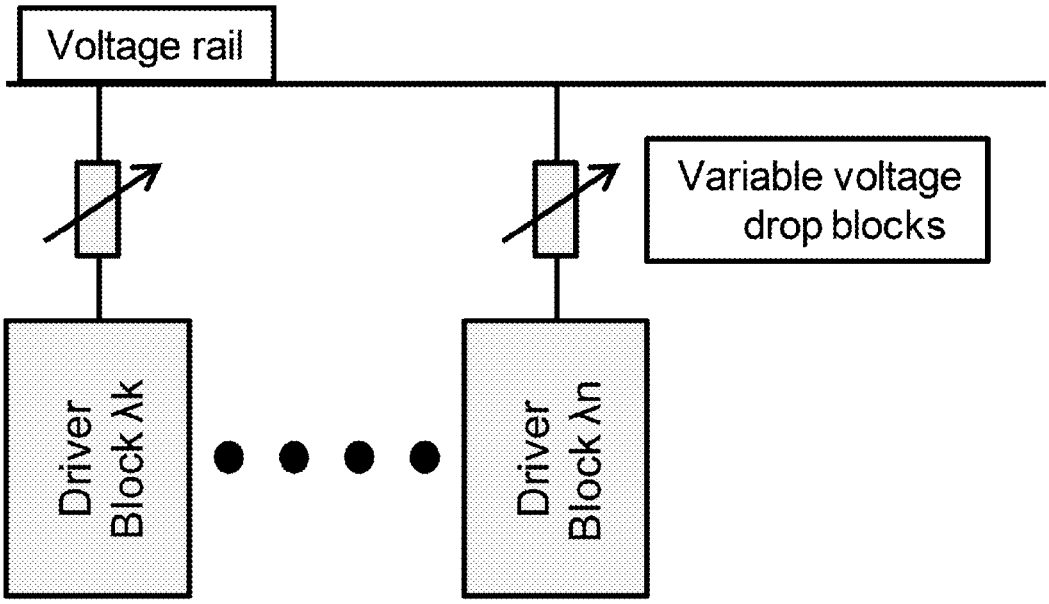

Voltage rail
Variable voltage drop blocks
Driver Block λk
Driver Block λn

Fig. 13

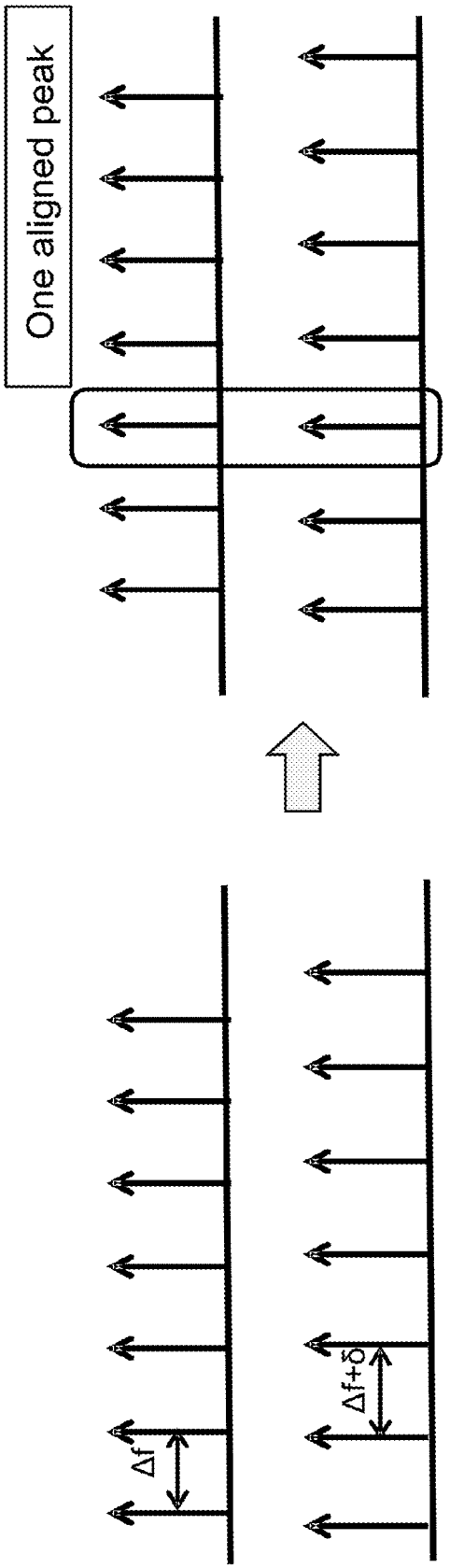


Fig. 14

BUILT-IN REDUNDANCY SCHEME FOR COMMUNICATION SYSTEM ON CHIP

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application No. 61/845,329, filed Jul. 11, 2013, commonly assigned and incorporated by reference herein for all purposes.

BACKGROUND OF THE INVENTION

The present invention relates to telecommunication techniques. More particularly, the present invention provides an integrated electrical optics multiple chip module and methods.

Over the last few decades, the use of communication networks exploded. In the early days Internet, popular applications were limited to emails, bulletin board, and mostly informational and text-based web page surfing, and the amount of data transferred was usually relatively small. Today, Internet and mobile applications demand a huge amount of bandwidth for transferring photo, video, music, and other multimedia files. For example, a social network like Facebook processes more than 500 TB of data daily. With such high demands on data and data transfer, existing data communication systems need to be improved to address these needs.

Over the past, there have been many types of communication systems and methods. Unfortunately, they have been inadequate for various applications. Therefore, improved communication systems and methods are desired.

BRIEF SUMMARY OF THE INVENTION

The present invention relates to telecommunication techniques. More specifically, various embodiments of the present invention provide a communication interface that is configured to transfer data at high bandwidth over optical communication networks. In certain embodiments, the communication interface is used by various devices, such as spine switches and leaf switches, within a spine-leaf network architecture, which allows large amount of data to be shared among servers.

In modern electrical interconnect systems, high-speed serial links have replaced parallel data buses, and serial link speed is rapidly increasing due to the evolution of CMOS technology. Internet bandwidth doubles almost every two years following Moore's Law. But Moore's Law is coming to an end in the next decade. Standard CMOS silicon transistors will stop scaling around 5 nm. And the internet bandwidth increasing due to process scaling will plateau. But Internet and mobile applications continuously demand a huge amount of bandwidth for transferring photo, video, music, and other multimedia files. This disclosure describes techniques and methods to improve the communication bandwidth beyond Moore's law.

Serial link performance is limited by the channel electrical bandwidth and the electronic components. In order to resolve the inter-symbol interference (ISI) problems caused by bandwidth limitations, we need to bring all electrical components as close as possible to reduce the distance or channel length among them. Stacking chips into so-called 3-D ICs promises a one-time boost in their capabilities, but it's very expensive. Another way to achieve this goal in this disclosure is to use multiple chip module technology.

In an example, an alternative method to increase the bandwidth is to move the optical devices close to electrical device. Silicon photonics is an important technology for moving optics closer to silicon. In this patent application, we will disclose a high speed electrical optics multiple chip module device to achieve terabits per second speed, as well as variations thereof.

In an alternative example, the present invention includes an integrated system on chip device. The device is configured on a single silicon substrate member. The device has a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. The device has an input/output block provided on the substrate member and coupled to the data input/output interface. In an example, the input/output block comprises a Serializer/Deserializer (SerDes) block, a clock data recovery (CDR) block, a compensation block, and an equalizer block, among others. The device has a signal processing block provided on the substrate member and coupled to the input/output block. In an example, the signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. The device has a driver module provided on the substrate member and coupled to the signal processing block. In an example, the driver module is coupled to the signal processing block using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. In an example, the device has a receiver module comprising a trans-impedance amplifier (TIA) block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input/output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, among others. The device has a communication interface coupled to the communication block. The device has a control block provided on the substrate member and coupled to the communication block.

In an example, the signal processing block comprises a forward error correction (FEC) block, a digital signal processing block, a framing block, a protocol block, and a redundancy block, among others. The driver module is selected from a current drive or a voltage driver in an example. In an example, the driver module is a differential driver or the like. In an example, the silicon photonics device is selected from an electro absorption modulator (EAM) or electro optic modulator (EOM), or a Mach-Zehnder modulator (MZM). In an example, the amplified modulation format is selected from non-return to zero (NRZ) format or pulse amplitude modulation (PAM) format. In an example, the phase modulation format is selected from binary phase shift keying (BPSK) or nPSK. In an example, the phase/amplitude modulation is quad amplitude modulation (QAM). In an example, the silicon photonic device is configured to convert the output data into an output transport data in a wave division multiplexed (WDM) signal. In an example, the control block is configured to initiate a laser bias or a modulator bias. In an example, the control block is configured for laser bias and power control of the silicon photonics device. In an example, the control block is configured with a thermal tuning or carrier tuning device

each of which is configured on the silicon photonics device. In an example, the SerDes block is configured to convert a first data stream of N into a second data stream of M.

In an example, the invention provides an integrated system on chip device. The device has a single silicon substrate member and a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. In an example, the device has an input/output block provided on the substrate member and coupled to the data input/output interface. The input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. The device has a signal processing block provided on the substrate member and coupled to the input/output block. In an example, the signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. In an example, the device has a driver module provided on the substrate member and coupled to the signal processing block. The driver module is coupled to the signal processing block using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. The driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format in an example. The device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input/output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block and the signal processing block, the driver block, and the receiver block, and others, although there may be variations. In an example, the device has a communication interface coupled to the communication block and a control block provided on the substrate member and coupled to the communication block. In an example, the control block is configured to receive and send instruction(s) in a digital format to the communication block and being configured to receive and send signals in an analog format to communicate with the silicon photonics device.

In an example, the present invention provides a monolithically integrated system on chip device configured for a multi-rate and selected format of data communication. In an example, the device has a single silicon substrate member. The device has a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. In an example, the data input/output interface is configured for number of lanes numbered from four to one hundred and fifty. The device has an input/output block provided on the substrate member and coupled to the data input/output interface, which has a SerDes block, a CDR block, a compensation block, and an equalizer block. In an example, the SerDes block is configured to convert a first data stream of N into a second data stream of M. In an example, each of the first data stream has a first predefined data rate at a first clock rate and each of the second data stream having a second predefined data rate at a second clock rate. As used herein the terms "first" and "second" do not necessarily imply order and shall be construed broadly according to ordinary meaning. In an example, the device has a signal processing block provided on the substrate member and coupled to the input/output block. The signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol in an example. The device has a driver module provided on the substrate member and coupled to the signal processing block. In an example, the driver module is coupled to the signal processing block using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. The device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and is configured to the signal processing block to communicate information to the input/output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, and others, although there can be variations. In an example, the device has a communication interface coupled to the communication block and a control block provided on the substrate member and coupled to the communication block.

In an example, the present invention provides a monolithically integrated system on chip device configured for a multi-rate and selected format of data communication. In an example, the device has a single silicon substrate member. The device has a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. In an example, the data input/output interface is configured for number of lanes numbered from four to one hundred and fifty, although there can be variations. In an example, the device has an input/output block provided on the substrate member and coupled to the data input/output interface. In an example, the input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. In an example, the SerDes block is configured to convert a first data stream of X into a second data stream of Y, where X and Y are different integers. Each of the first data stream has a first predefined data rate at a first clock rate and each of the second data stream has a second predefined data rate at a second clock rate in an example. In an example, the device has a signal processing block provided on the substrate member and coupled to the input/output block. In an example, the signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. In an example, the device has a driver module provided on the substrate member and coupled to the signal processing block. In an example, the driver module is coupled to the signal processing block using a uni-directional multi-lane bus configured with N lanes, whereupon N is greater than M such that a difference between N and M represents a redundant lane or lanes. In an example, the device has a mapping block configured to associate the M lanes to a plurality of selected laser devices for a silicon photonics device. The device also has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to the silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. In an example, the device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input/output block for transmission through the data input/output inter-

face. The device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, among others. The device has a communication interface coupled to the communication block and a control block provided on the substrate member and coupled to the communication block.

In an example, the device has an integrated system on chip device. The device has a single silicon substrate member and a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. In an example, the device has an input/output block provided on the substrate member and coupled to the data input/output interface. In an example, the input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. The device has a signal processing block provided on the substrate member and coupled to the input/output block. The signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. The device has a driver module provided on the substrate member and coupled to the signal processing block. In an example, the driver module is coupled to the signal processing block using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. In an example, the device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input/output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, and among others. The device has a communication interface coupled to the communication block and a control block provided on the substrate member and coupled to the communication block. In an example, the device has a variable bias block configured with the control block. In an example, the variable bias block is configured to selectively tune each of a plurality of laser devices provided on the silicon photonics device to adjust for at least a wavelength of operation, a fabrication tolerance, and an extinction ratio.

In an example, the present invention provides an integrated system on chip device having a self test using a loop back technique. In an example, the device has a self-test block provided on the substrate, the self test block being configured to receive a loop back signal from at least one of the digital signal processing block, the driver module, or the silicon photonics device. In an example, the self test block comprises a variable output power switch configured to provide a stress receiver test from the loop back signal.

In an example, the invention provides an integrated system on chip device having a redundant laser or lasers configured for each channel. In an example, the device has a plurality of laser devices configured on the silicon photonics device. At least a pair of laser devices is associated with a channel and coupled to a switch to select one of the pair of laser devices to be coupled to an optical multiplexer to provide for a redundant laser device.

In an example, the present invention provides an integrated system on chip device having a built-in self test technique. In an example, the device has a self test block configured on the silicon photonics device and to be operable during a test operation. In an example, the self test block comprises a broad band source configured to emit electromagnetic radiation from 1200 nm to 1400 nm or 1500 to 1600 nm to a multiplexer device. In an example, the broad band source can be an LED or other suitable device. The device also includes a self test output configured to a spectrum analyzer device external to the silicon photonics device.

The present invention achieves these benefits and others in the context of known memory technology. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The following diagrams are merely examples, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this process and scope of the appended claims.

FIG. **1** is a simplified diagram of a single hybrid die (Both electrical and optics devices are fabricated on a single hybrid die) according to an embodiment of the present invention.

FIG. **2** is a simplified diagram of a multi-chip module according to an embodiment of the present invention.

FIG. **2**A is a simplified diagram of an exemplary hybrid silicon photonics device.

FIG. **3** is a simplified diagram of an electrical silicon die block according to an embodiment of the present invention.

FIG. **4** is a simplified diagram of high speed serial link block according to an embodiment of the present invention.

FIG. **5** is a simplified diagram of a digital processing/signal pre-distortion block according to an embodiment of the present invention.

FIG. **6** is a simplified diagram of an electrical laser driver and TIA block diagram according to an embodiment of the present invention.

FIG. **7** is a simplified diagram of a silicon photonic block diagram according to an embodiment of the present invention.

FIG. **8** is a simplified block diagram of a multi-chip module according to an alternative embodiment of the present invention.

FIG. **9** is a simplified block diagram of data flow according to an embodiment of the present invention.

FIG. **10** is a simplified diagram illustrating a redundant laser configuration at a drive stage according to an embodiment of the present invention.

FIG. **11** is a simplified diagram illustrating a built-in self test using an optical loop back according to an embodiment of the present invention.

FIG. **12** is a simplified diagram illustrating a built-in self test configured for optical testing according to an embodiment of the present invention.

FIG. **13** is a simplified diagram illustrating a variable bias for optical elements configured within a silicon photonic device according to an embodiment of the present invention.

FIG. **14** is a simplified diagram illustrating wavelength tuning configured to silicon photonic device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

This present invention relates to telecommunication techniques. More specifically, various embodiments of the present invention provide a communication interface that is configured to transfer data at high bandwidth over optical communication networks. In certain embodiments, the communication interface is used by various devices, such as spine switches and leaf switches, within a spine-leaf network architecture, which allows large amount of data to be shared among servers.

In the last decades, with advent of cloud computing and data center, the needs for network servers have evolved. For example, the three-level configuration that have been used for a long time is no longer adequate or suitable, as distributed applications require flatter network architectures, where server virtualization that allows servers to operate in parallel. For example, multiple servers can be used together to perform a requested task. For multiple servers to work in parallel, it is often imperative for them to be share large amount of information among themselves quickly, as opposed to having data going back forth through multiple layers of network architecture (e.g., network switches, etc.).

Leaf-spine type of network architecture is provided to better allow servers to work in parallel and move data quickly among servers, offering high bandwidth and low latencies. Typically, a leaf-spine network architecture uses a top-of-rack switch that can directly access into server nodes and links back to a set of non-blocking spine switches that have enough bandwidth to allow for clusters of servers to be linked to one another and share large amount of data.

In a typical leaf-spine network today, gigabits of data are shared among servers. In certain network architectures, network servers on the same level have certain peer links for data sharing. Unfortunately, the bandwidth for this type of set up is often inadequate. It is to be appreciated that embodiments of the present invention utilizes PAM (e.g., PAM8, PAM12, PAM16, etc.) in leaf-spine architecture that allows large amount (up terabytes of data at the spine level) of data to be transferred via optical network.

The following description is presented to enable one of ordinary skill in the art to make and use the invention and to incorporate it in the context of particular applications. Various modifications, as well as a variety of uses in different applications will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to a wide range of embodiments. Thus, the present invention is not intended to be limited to the embodiments presented, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

In the following detailed description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without necessarily being limited to these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

The reader's attention is directed to all papers and documents which are filed concurrently with this specification and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference. All the features disclosed in this specification, (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

Furthermore, any element in a claim that does not explicitly state "means for" performing a specified function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. Section 112, Paragraph 6. In particular, the use of "step of" or "act of" in the Claims herein is not intended to invoke the provisions of 35 U.S.C. 112, Paragraph 6.

Please note, if used, the labels left, right, front, back, top, bottom, forward, reverse, clockwise and counter clockwise have been used for convenience purposes only and are not intended to imply any particular fixed direction. Instead, they are used to reflect relative locations and/or directions between various portions of an object.

FIG. **1** is a simplified diagram of a single hybrid die (Both electrical and optics devices are fabricated on a single hybrid die) according to an embodiment of the present invention. In an example, the present device comprises a single hybrid communication module made of silicon material. The module comprises a substrate member having a surface region, an electrical silicon chip overlying a first portion of the surface region, an silicon photonics device overlying a second portion of the surface region, a communication bus coupled between the electrical silicon chip and the silicon photonics device, an optical interface coupled to the silicon photonics device, and an electrical interface coupled to the electrical silicon die.

FIG. **2** is a simplified diagram of a multi-chip module according to an embodiment of the present invention. In an example, the present device comprises a single hybrid communication module. The module comprises a substrate member having a surface region, which can be a printed circuit board or other member. The module comprises an electrical silicon chip overlying a first portion of the surface region, a silicon photonics device overlying a second portion of the surface region, a communication bus coupled between the electrical silicon chip and the silicon photonics device, an optical interface coupled to the silicon photonics device, and an electrical interface coupled to the electrical silicon die.

As shown in FIG. **1**, the single hybrid die includes a hybrid silicon photonics device having an electrical circuit for processing and control and a silicon photonics module. In an example, the hybrid silicon photonics device is described in U.S. Pat. No. 8,380,033, in the name of Fang, et al. issued Feb. 19, 2013, hereby incorporated by reference. FIG. **2**A shows a simplified block diagram of an exemplary hybrid silicon photonics device.

In this example, electro-optic device **200** includes a silicon semiconductor slab including silicon top layer **201**, vertical confinement layer **202** and silicon substrate **203**. Alternatively, substrate layer **203** may be a diamond substrate, a glass substrate, or any functional equivalent. Vertical confinement layer **202** may be formed of any dielectric material suitable for confining an optical mode (e.g., layer **201** may be a silicon dioxide layer, a silicon nitride layer, or any functionally equivalent insulating layer with a refractive index lower than silicon top layer **201**).

Device **200** further includes a III-V semiconductor slab including p-type layer **208**, active layer **209** and n-type layer **210** (thereby forming a P-I-N diode). The term "p-type layer," as used herein, describes a layer comprising a material that has more positive carriers (i.e., holes) than negative carriers (i.e., electrons). The term "n-type layer," as used herein, describes a layer comprising a material that has more negative carriers than positive carriers.

Alternatively, layer **208** may be an n-type layer, and layer **210** may be a p-type layer. Or, layers **208** and **210** may be

n-type layers, while active region **209** may include a tunnel junction to convert n-type majority carriers to p-type majority carriers. This avoids the associated optical and microwave loss of p-type materials due to the use of p-dopants.

III-V semiconductor materials have elements that are found in group III and group V of the periodic table (e.g., Indium Gallium Arsenide Phosphide, Gallium Indium Arsenide Nitride). The carrier dispersion effects of III-V based materials may be significantly higher than in silicon based materials for bandgaps closer to the wavelength of the light being transmitted or modulated, as electron speed in III-V semiconductors is much faster than that in silicon. In addition, III-V materials have a direct bandgap which is required for the most efficient creation of light from electrical pumping. Thus, III-V semiconductor materials enable photonic operations with an increased efficiency over silicon for both generating light and modulating the refractive index of light.

Active layer **209** is of a III-V semiconductor with high electro-optic efficiency, i.e., the absorption coefficient (i.e., the imaginary portion of the complex refractive index) and the refractive index (i.e., the real portion of the complex refractive index) of active layer **209** is easily affected by either the Franz Kheldysh effect if active layer **209** comprises bulk material (e.g., intrinsic Indium Gallium Arsenide Phosphide or Indium Aluminum Gallium Arsenide or the Quantum Confined Stark Effect if active layer **209** comprises multiple quantum wells.

Optical waveguide **250** is formed by ridge **260** (which is "bolded" or "thicker" in the figure for illustrative purposes only), including ridge sides **261** and **262**. It is clear that in this embodiment, waveguide **250** is formed by features in the III-V region of device **200** as opposed to being formed by features in the silicon region of the device, wherein waveguide is formed by voids included in silicon top region. Thus, the silicon and III-V regions of device **200** have a greater contact area than devices in the prior art (where layer **210** was continuously coupled to layer **201**).

Overclad regions **207** may be formed on the device to improve mechanical stability, and may be of any material used to form vertical confinement layer **202** or any material with a lower refractive index than layer **208**. Overclad regions **207** further provide vertical optical confinement and passivation as described below. The areas adjacent to ridge sides **261** and **262** provide optical confinement if left as voids (i.e., areas comprising air), but that forming overclad regions **207** provides for mechanical stability in addition to optical confinement.

Thus, optical mode **213** is vertically confined by vertical confinement layer **202**, ridge **260** and overclad regions **207** while being laterally confined by ridge sides **261** and **262**. Said ridge sides also confine injection current from electrode **206** towards the portion of active layer **209** that overlaps optical mode **213**. The need for the etched regions and implanted regions is eliminated in the example shown above.

It is understood that the optical device of FIG. **2**A may be used to amplify, modulate or detect light transmitted through the optical waveguide of the device by applying an electrical difference to complimentary electrodes **206** and **212** to either forward bias (i.e., for amplification) or reverse bias (i.e., for modulation or detection) the structure. The complex refractive index (i.e., at least one of the real and the imaginary refractive index) of at least the portion of active layer **209** included in optical mode **213** changes based on an electrical difference (e.g., electrical voltage, electrical field) applied to electrodes **206** and **212**. These changes to the refractive index (or indexes) are proportional to the strength of the electrical difference applied to electrodes **206** and **212**.

In this example, electrodes **212** are coupled to n-type layer **210**. Thus, it is to be understood that there is no electrical conduction through silicon top layer **201**. As opposed to variations where electrical conduction does occur through the silicon top layer of a device, resistance is high as it determined by thin layer **210**; however, there are less processing steps needed to create device **200** and no conductive bond is required to couple the silicon region with the III-V region (i.e., no conductive bond is required to couple layers **210** and **201**).

Other examples of silicon photonic devices are manufactured by Intel Corporation of Santa Clara, Calif., Skorpis Technology, Inc. 5600 Eubank Blvd. NE Suite 200, Albuquerque, N. Mex. 87111, Luxtera, Inc. of 2320 Camino Vida Roble, Carlsbad, Calif. 92011, Mellanox Technologies, Inc. 350 Oakmead Parkway, Suite 100 Sunnyvale, Calif. 94085, and am Lightwire, Inc. Headquartered in Allentown, Pa. (now Cisco Systems, Inc., Corporate Headquarters, 170 West Tasman Dr., San Jose, Calif. 95134) among others.

FIG. **3** is a simplified diagram of an electrical silicon die block according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. In an embodiment, the electrical silicon die block is an electrical signal processing block that connects a low speed electrical interface to a high speed optical interface. There are several elements to this block diagram. As shown, the electrical silicon die block includes a high speed serial link **310**, a digital signal processing/pre-distortion unit **320**, and a laser modulator driver and TIA unit **330**. The high speed serial link **310** includes an input/output block having an RX (receiving) functional unit and a TX (transmitting) function unit coupled to a phase lock loop circuit. For example, the TX function unit drives the loopback signals that are processed by the RX functional unit. Using the high speed serial link **310**, the data first is able to be converted from the many parallel streams of lower speed data into a high speed serial stream (there may be more than one such high speed stream depending on the total data rate). The digital signal processing/pre-distortion unit **320** is configured to process or convert digital electrical signal back and forth to optical signal and conduct all signal modulation, error encoding/decoding, and signal distortion compensation. The high speed streams converted by the high speed serial link **310** are then encoded and digitally compensated to account for distortions in the transmit and receive paths. The final interface to the optical components is achieved via the modulator driver (transmit path) and the transimpedance amplifier (receive path). The laser modulator driver and TIA unit **330** is configured to control the optical device (such as the optics silicon photonics die on the part of the multi-chip module in FIG. **2**). In a specific embodiment, the electrical silicon die block is a single hybrid die as part of the multi-chip module shown in FIG. **2**.

FIG. **4** is a simplified diagram of high speed serial link block according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown, the high speed serial link block provides details of the signal interface between the high speed optical and the lower speed electrical sides. In an embodiment, the high speed serial link block comprises multiple Bits Flash Samplers **410** and an All digital SerDes core unit **420** powered under a low Vdd power supply. The samplers **410** are part of RX functional unit of the input/output block **310**. The all digital SerDes core unit **420** comprises an all digital phase

lock loop (PLL) block **422**, a fast lock CDR block **424**, and Digital offset calibrations and logics block **426**, also belonging to the RX functional unit (**310** of FIG. **3**). In another embodiment, the high speed serial link block is an electrical input/output block provided on either a single chip or a silicon die of package substrate member and coupled to the data input/output interface. Some of the essential components of the electrical input/output block are CDR (clock and data recovery circuits), PLL (phase lock loops), and SerDes (Serializers and Deserializers). In an example, the input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. The output of equalizer includes receiver input. These circuits in combination convert multiple streams of input data (electrical side) to fewer streams of output data (optical side). These circuits also need to be calibrated and controlled to operate correctly.

FIG. **5** is a simplified diagram of a digital processing/signal pre-distortion block according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown, the digital processing/signal pre-distortion block comprises at least an Error Encoding/Decoding block **510**, an Optical Distortion/Electrical Compensation (EDC) block **520**, and a Modulation Conversion block **530**. In an example, it shows the details of a possible implementation of the electronic processing blocks in the transmit and receive paths. In an alternative embodiment, some of those blocks may be configured differently in the transmit versus the receive path. One of the essential blocks is the Error Encoding/Decoding block **510** which performs data error detection/correction coding. As additional data bits are added to blocks of signal data in such a way that when errors occur they may be correctable in the receive path. Modern error control codes are sophisticated that they can correct, e.g., up to 1 error in every 100 bits with modest data overhead and latency. The optical distortion compensation block **520** helps compensate for impairments in the optical and electrical transmission paths. These could include compensation of, e.g., bandwidth limitations and inter-symbol interference. The modulation conversion block **530** codes and decodes the multi-level higher-order modulation signals that are used at the transmitter and receiver, and converts them to the simple two-level NRZ format used in the lower speed interfaces.

In an embodiment, the Error Encoding/Decoding block **510** includes an Encoding/Decoding block **511**, a Framing block **512**, a Protocol block **513**, and a Redundancy block **514**. The electrical data signals are transmitted in terms of modulate electromagnetic waves with varying voltage. The encoding/decoding block **511** is to encode binary data onto the signals. Data error detection/correction coding may include Checksum, Cyclic Redundancy Check (CRC), Forward Error Correction (FEC), and others. Corresponding decoding schemes are used with one or more being determined and selected in the Protocol block **513**. In the Framing block **512**, the data signal is broken up into sequence of bits in multiple units, each unit is a frame. For example, starting and ending characters (tags) are used to mark boundaries of frame. In another example, bit strings may be used instead of character sequences to delineate frames. During the error detection and correction, redundancy block **514** adds redundancy to transmitted information using a predetermined algorithm. The redundant bits are complex functions of the original data bits. Bits are sent multiple times, because an error may appear in any of the samples transmitted. FEC codes generally detect the last set of bits to determine the decoding of a small handful of bits.

In another embodiment, the Optical Distortion/Electrical Compensation (EDC) block **520** further is made of a Digital Signal Processing block **521** and a Compensation block **522**. The modulation conversion block **530** is configured into a Slicers block **531** and an Analog to Digital Converters block **532**.

FIG. **6** is a simplified diagram of an electrical laser driver and TIA block diagram according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown, the top part circuit (A) of an electrical laser driver and TIA block shows a driver circuit for the modulator and the receiver circuit for a photo diode detector (to be shown in FIG. **7** below). The electrical output of the top circuit (A) is used to drive the modulator. The modulator imprints the electrical signal input on to the optical carrier. The output of the photo diode detector is the input to the bottom part circuit (B) of the electrical laser driver and TIA block. This circuit converts the current signal from the photo diode detector into a voltage signal which can then be processed by other circuits. In an example, the electrical laser driver and TIA block is block **330** included in the electrical silicon die block shown in FIG. **3**.

FIG. **7** is a simplified diagram of a silicon photonic block diagram according to an embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. As shown, in an embodiment, a silicon photonic block **700** includes a laser source **710**, a laser modulator **720**, a control loop **730**, and one or more photo detectors **740**. In a specific embodiment, the silicon photonic block **700** includes common blocks of an optical sub-system including control loops. The transmit path of the optical sub-system includes a laser source **710** which can be selected from a CW (continuous wave) DFB (distributed feedback) laser among others. The laser source **710** provides the optical carrier. The output from the laser source **710** is optically coupled into the laser modulator **720**. The electrical data is converted to optical via the modulator for modulating the optical signal directly from the laser source **710**. The modulator **720** may be an electro-absorption modulator or a Mach-Zehnder (MZ) modulator, or others depending on embodiments. The output signal from the modulator **720** is then coupled to a fiber (not shown) for external transmission. The receive path of the optical sub-system includes the optical signal from the fiber coupled into one or more photo diode detectors **740**. The photo diode detector **740** converts the optical data into electrical data. The control loops **730** are needed to correctly bias the laser source **710**, the modulator **720**, and the one or more photo diode detectors **740**. The bias control signals may include current or voltage outputs used to setup the laser source, modulator, and the photo diode detector correctly. The control output signals may also be continually adjusted using the feedback from the devices themselves.

FIG. **8** is a simplified block diagram of a multi-chip module according to an alternative embodiment of the present invention. As shown, the present invention includes an integrated system on chip device. The device is configured on a single silicon substrate member. The device has a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. The device has an input/output block provided on the substrate member and

coupled to the data input/output interface. In an example, the input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. The device has a signal processing block provided on the substrate member and coupled to the input/output block. In an example, the signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. The device has a driver module provided on the substrate member and coupled to the signal processing block. In an example, the driver module is coupled to the signal processing blocking using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. In an example, the device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, among others. The device has a communication interface coupled to the communication block. The device has a control block provided on the substrate member and coupled to the communication block.

In an example, the signal processing block comprises a FEC block, a digital signal processing block, a framing block, a protocol block, and a redundancy block, among others. The driver module is selected from a current drive or a voltage driver in an example. In an example, the driver module is a differential driver or the like. In an example, the silicon photonics device is selected from an electro absorption modulator or electro optic modulator, or a Mach-Zehnder. In an example, the amplified modulation format is selected from NRZ format or PAM format. In an example, the phase modulation format is selected from BPSK or nPSK. In an example, the phase/amplitude modulation is QAM. In an example, the silicon photonic device is configured to convert the output data into an output transport data in a WDM signal. In an example, the control block is configured to initiate a laser bias or a modulator bias. In an example, the control block is configured for laser bias and power control of the silicon photonics device. In an example, the control block is configured with a thermal tuning or carrier tuning device each of which is configured on the silicon photonics device. In an example, the SerDes block is configured to convert a first data stream of N into a second data stream of M.

FIG. **9** is a simplified block diagram of data flow according to an embodiment of the present invention. As show is a stream of incoming data, which processed through multiple blocks. The blocks include, among others, forward error correction (FEC), and other encoding, Digital Signal Processing (DSP) multi-level coding, pre-compression, and digital to analog coding. The blocks also include non-DSP forward error correction, and a block corresponding to a laser diode or driver, among others. In an example, in the absence of a FEC from a host process, techniques include use of CDR2 type FEC, which is internal to the CMOS chip. In an example, FEC can be striped across each or all of data lanes. FEC is a technique used to enhance data reliability by introducing redundant data, called error correcting code, prior to data transmission or storage. FEC provides the receiver with the ability to correct errors without a reverse channel to request the retransmission of data. The redundant bits are configured as certain functions of the original data bits. Bits are sent multiple times, because an error may appear in any of the samples transmitted. FEC codes generally detect the last set of bits to determine the decoding of a small handful of bits. Of course, there can be variations, modifications, and alternatives.

FIG. **10** is a simplified diagram illustrating a redundant laser configuration at a drive stage according to an embodiment of the present invention. In an example, the invention provides an integrated system-on-chip device as a fully redundant system having a redundant laser or lasers configured for each channel. In an example, the device has a plurality of laser devices configured on the silicon photonics device. At least a pair of laser devices is associated with a channel and coupled to a switch to select one of the pair of laser devices to be coupled to an optical multiplexer to provide for a redundant laser device. The worst case is to have 2 times total number of wavelengths with twice in chip size. In an embodiment, the switch is a Mach-Zehnder Interferometer (MZI) switch used to switch between $\lambda 1$ and $\lambda 1'$. Or it could be a passive coupler. In another embodiment, it preserves the size of the wavelength multiplexer so that no additional λ channels are needed. Note, the integrated system-on-chip device doesn't have to operate $\lambda 1'$ until needed, therefore no power consumption penalty is applied.

FIG. **11** is a simplified diagram illustrating a built-in self test using an optical loop back according to an embodiment of the present invention. As shown are a TX multiplexer and an RX multiplexer for a silicon photonics device. In an example, the present invention provides an integrated system on chip device having a self test using a loop back technique. In an example, the device has a self-test block provided on the substrate. In an example, the self test block is configured to receive a loop back signal from at least one of the signal processing block, the driver module, or the silicon photonics device. In an example, the self test block comprises a variable output power switch configured to provide a stress receiver test from the loop back signal. Also shown is an isolation switch between RX and TX.

In an example, the present technique allows a loop back test capability on the device, which is now a silicon photonic application specific integrated circuit or a communication system on chip device, as described. In an example, the technique is provided for diagnostic and setup during power up sequence. In an example, an optical tap coupler on the output side connected to the input side as shown. In an example as shown, x (e.g., <10%) is selected to reduce and/or minimize an impact an output power as well an impact at the input power given that input power is generally much lower than the output power. In an example, to prevent crosstalk in the present loop back path, an isolation switch has been configured as shown. In an example, without the isolation switch there is undesirably direct crosstalk between the output and input as shown. In an example, about 30 dB isolation is included to prevent coherent crosstalk. Of course, there can be variations.

FIG. **12** is a simplified diagram illustrating a built-in self test configured for optical testing according to an embodiment of the present invention. In an example, the present invention provides an integrated system on chip device having a built-in self test technique. As shown are a TX multiplexer and an RX multiplexer for a silicon photonics device. A broad band source is coupled to each of the multiplexers. Multiple sources can also be included. In an example, the device has a self test block configured on the silicon photonics

device and to be operable during a test operation. In an example, the self test block comprises a broad band source configured to emit electromagnetic radiation from 1200 nm to 1400 nm or 1500 to 1600 nm to a multiplexer device. In an example, the broad band source can be an LED or other suitable device. The device also includes a self test output configured to a spectrum analyzer device external to the silicon photonics device. In an example, the technique can be provided during a calibration process. That is, if after calibration, a center λ of each multiplexer changed, the present technique including built-in light source will quantify or indicate the change in an example. In an example, the broadband source in silicon photonics is a light source with no optical feedback, although there can be variations.

FIG. **13** is a simplified diagram illustrating a variable bias for optical elements configured in a silicon photonic device according to an embodiment of the present invention. As shown are transfer curves provided for optical elements. In an example, the device has an integrated system on chip device having a capability selectively adjust each optical modulator to accommodate for fabrication tolerances, wavelength operation, and/or extinction ratio, among other parameters. The device has a single silicon substrate member and a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol. In an example, the device has an input/output block provided on the substrate member and coupled to the data input/output interface. In an example, the input/output block comprises a SerDes block, a CDR block, a compensation block, and an equalizer block, among others. The device has a signal processing block provided on the substrate member and coupled to the input/output block. The signal processing block is configured to the input/output block using a bi-direction bus in an intermediary protocol. The device has a driver module provided on the substrate member and coupled to the signal processing block.

In an example, the driver module is coupled to the signal processing blocking using a uni-directional multi-lane bus. In an example, the device has a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to a silicon photonics device. In an example, the driver interface is configured to transmit output data in either an amplitude modulation format or a combination of phase/amplitude modulation format or a phase modulation format. In an example, the device has a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using predefined modulation format, and configured to the signal processing block to communicate information to the input output block for transmission through the data input/output interface. In an example, the device has a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block, and among others. The device has a communication interface coupled to the communication block and a control block provided on the substrate member and coupled to the communication block.

In an example, the device has a variable bias block configured with the control block. In an example, the variable bias block is configured to selectively tune each of a plurality of laser devices provided on the silicon photonics device to adjust for at least a wavelength of operation, a fabrication tolerance, and an extinction ratio. As shown is a plurality of driver blocks. Each of the driver blocks is coupled to a voltage rail, and is configured with a variable voltage device to selectively tune each of the laser devices. In an example, each of the laser devices can be configured with an optical modulator(s) such as electro-absorption modulators, electro-optical modulators, among others, which often couple to a direct current power or bias. In an example, the DC bias is a function of wavelength of operation and also of fabrication tolerances, among other factors. In an example, the present bias circuitry accommodates and/or corrects for any bias variations, while desirably controlling power. Of course, there can be variations, modifications, and alternatives.

FIG. **14** is a simplified diagram illustrating wavelength tuning configured to silicon photonic device according to an embodiment of the present invention. In an example, the present tunable laser uses a set of rings with resonant frequencies that a slightly different. In an example, the technique use a vernier effect to tune the laser over a wide frequency range—limited by the bandwidth of the gain region. In an example, the vernier desirably would be held in lock with respect to one another. In an example, the technique uses a dither frequency on one of the biases (e.g., heater) and lock the ring to the maximum transmission of the second ring, although there can be variations. As shown, resonant combs are generally misaligned in an example. When thermally tuned, techniques can be used to selectively align one of the combs to another comb or spatial reference. In an example, to maintain alignment, the technique dithers the signal to one of the rings. Of course, there can be variations, alternatives, and modifications.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A monolithically integrated system on chip device configured for a multi-rate and selected format of data communication, the device comprising:

a single silicon substrate member;

a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol, the data input/output interface being configured for a number of lanes numbered from four to one hundred and fifty;

an input/output block provided on the substrate member and coupled to the data input/output interface, the input/output block comprising a SerDes block, a CDR block, a compensation block, and an equalizer block, the SerDes block being configured to convert a first data stream of X into a second data stream of Y, each of the first data stream having a first predefined data rate at a first clock rate and each of the second data stream having a second predefined data rate at a second clock rate;

a signal processing block provided on the substrate member and coupled to the input/output block, the signal processing block configured to the input/output block using a bi-direction bus in an intermediary protocol;

a driver module provided on the substrate member and coupled to the signal processing block, the driver module coupled to the signal processing blocking using a uni-directional multi-lane bus configured with N lanes;

a mapping block configured to associate M lanes to a plurality of selected laser devices for a silicon photonics device, whereupon N is greater than M such that a difference between N and M represents a redundant lane or lanes;

a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to the silicon photonics device, the driver inter-

face comprising a slicer block and being configured to transmit output data in a multi-level pulse amplitude modulation (PAM) format;

a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using the multi-level pulse amplitude modulation format, and coupled to the signal processing block to communicate information to the input output block for transmission through the data input/output interface;

a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block;

a communication interface coupled to the communication block;

a control block provided on the substrate member and coupled to the communication block; and

a redundancy block configured to add at least a redundancy bit as a function of one or more data bits associated with data for data error detection and correction, wherein the redundancy block is configured for at least data error detection/correction coding selected from at least one of a Checksum or Cyclic Redundancy Check (CRC).

2. The device of claim **1** wherein the signal processing block comprises a digital signal processing block, a framing block, a protocol block, and the redundancy block.

3. The device of claim **1** wherein the driver module is selected from a current drive or a voltage driver.

4. The device of claim **1** wherein the driver module is a differential driver.

5. The device of claim **1** wherein the redundancy block is configured with redundant bits, the redundant bits are configured as complex functions of original data bits.

6. The device of claim **1** wherein the silicon photonic device is configured to convert the output data into an output transport data in a WDM signal.

7. The device of claim **1** wherein the control block is configured to initiate a laser bias or a modulator bias.

8. The device of claim **1** wherein the control block is configured for laser bias and power control of the silicon photonics device.

9. The device of claim **1** wherein the control block is configured with a thermal tuning or carrier tuning device each of which is configured on the silicon photonics device.

10. The device of claim **1** wherein the plurality of laser devices comprises a redundant laser device.

11. A monolithically integrated system on chip device configured for a multi-rate and selected format of data communication, the device comprising:

a single silicon substrate member;

a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol, the data input/output interface being configured for a number of lanes numbered from four to one hundred and fifty;

an input/output block provided on the substrate member and coupled to the data input/output interface, the input/output block comprising a SerDes block, a CDR block, a compensation block, and an equalizer block, the SerDes block being configured to convert a first data stream of X into a second data stream of Y, each of the first data stream having a first predefined data rate at a first clock rate and each of the second data stream having a second predefined data rate at a second clock rate;

a signal processing block provided on the substrate member and coupled to the input/output block, the signal processing block configured to the input/output block using a bi-direction bus in an intermediary protocol;

a driver module provided on the substrate member and coupled to the signal processing block, the driver module coupled to the signal processing blocking using a uni-directional multi-lane bus configured with N lanes;

a mapping block configured to associate M lanes to a plurality of selected laser devices for a silicon photonics device, whereupon N is greater than M such that a difference between N and M represents a redundant lane or lanes;

a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to the silicon photonics device, the driver interface comprising a slicer block and being configured to transmit output data in a multi-level pulse amplitude modulation (PAM) format;

a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using the multi-level pulse amplitude modulation format, and coupled to the signal processing block to communicate information to the input output block for transmission through the data input/output interface;

a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block;

a communication interface coupled to the communication block;

a control block provided on the substrate member and coupled to the communication block; and

a redundancy block configured to add at least a redundancy bit as a function of one or more data bits associated with data for data error detection and correction; and the function is configured as a complex function of the one or more data bits, wherein the redundancy block is configured for at least data error detection/correction coding selected from at least one of a Checksum or Cyclic Redundancy Check (CRC).

12. The device of claim **11** wherein the signal processing block comprises a digital signal processing block, a framing block, a protocol block, and the redundancy block.

13. The device of claim **11** wherein the driver module is selected from a current drive or a voltage driver or a differential driver.

14. The device of claim **11** wherein the redundancy block is configured with redundant bits, the redundant bits are configured as complex functions of original data bits.

15. The device of claim **11** wherein the plurality of laser devices comprises a redundant laser device.

16. A monolithically integrated system on chip device configured for a multi-rate and selected format of data communication, the device comprising:

a single silicon substrate member;

a data input/output interface provided on the substrate member and configured for a predefined data rate and protocol, the data input/output interface being configured for a number of lanes numbered from four to one hundred and fifty;

an input/output block provided on the substrate member and coupled to the data input/output interface, the input/output block comprising a SerDes block, a CDR block, a compensation block, and an equalizer block, the SerDes block being configured to convert a first data stream of X into a second data stream of Y, each of the first data stream having a first predefined data rate at a first clock

rate and each of the second data stream having a second predefined data rate at a second clock rate;

a signal processing block provided on the substrate member and coupled to the input/output block, the signal processing block configured to the input/output block using a bi-direction bus in an intermediary protocol;

a driver module provided on the substrate member and coupled to the signal processing block, the driver module coupled to the signal processing blocking using a uni-directional multi-lane bus configured with N lanes;

a mapping block configured to associate M lanes to a plurality of selected laser devices for a silicon photonics device, whereupon N is greater than M such that a difference between N and M represents a redundant lane or lanes;

a driver interface provided on the substrate member and coupled to the driver module and configured to be coupled to the silicon photonics device, the driver interface comprising a slicer block and being configured to transmit output data in a multi-level pulse amplitude modulation (PAM) format;

a receiver module comprising a TIA block provided on the substrate member and to be coupled to the silicon photonics device using the multi-level pulse amplitude modulation format, and coupled to the signal processing block to communicate information to the input output block for transmission through the data input/output interface;

a communication block provided on the substrate member and operably coupled to the input/output block, the signal processing block, the driver block, and the receiver block;

a communication interface coupled to the communication block;

a control block provided on the substrate member and coupled to the communication block; and

a redundancy block configured to add at least a redundancy bit as a function of one or more data bits associated with data for data error detection and correction; and the function is configured as a complex function of the one or more data bits,

wherein the redundancy block is configure for at least data error detection/correction coding selected from at least one of a Checksum or Cyclic Redundancy Check (CRC).

17. The device of claim **16** wherein the silicon photonic device is configured to convert the output data into an output transport data in a WDM signal; wherein the control block is configured to initiate a laser bias or a modulator bias; wherein the control block is configured for laser bias and power control of the silicon photonics device.

18. The device of claim **16** wherein the plurality of laser devices comprises a redundant laser device.

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